UNIT II

BIPOLAR JUNCTION TRANSISTOR

INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogues to vacuum triode and is comparatively smaller in size. It is used as amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

CONSTRUCTION OF BJT AND ITS SYMBOLS

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labeled as the Emitter (E), the Base (B) and the Collector (C) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. Active Region - the transistor operates as an amplifier and Ic = β.Ib
- 2. Saturation - the transistor is "fully-ON" operating as a switch and Ic = I(saturation)
- 3. Cut-off - the transistor is "fully-OFF" operating as a switch and Ic = 0

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type(fig 1).

Bipolar Transistor Construction

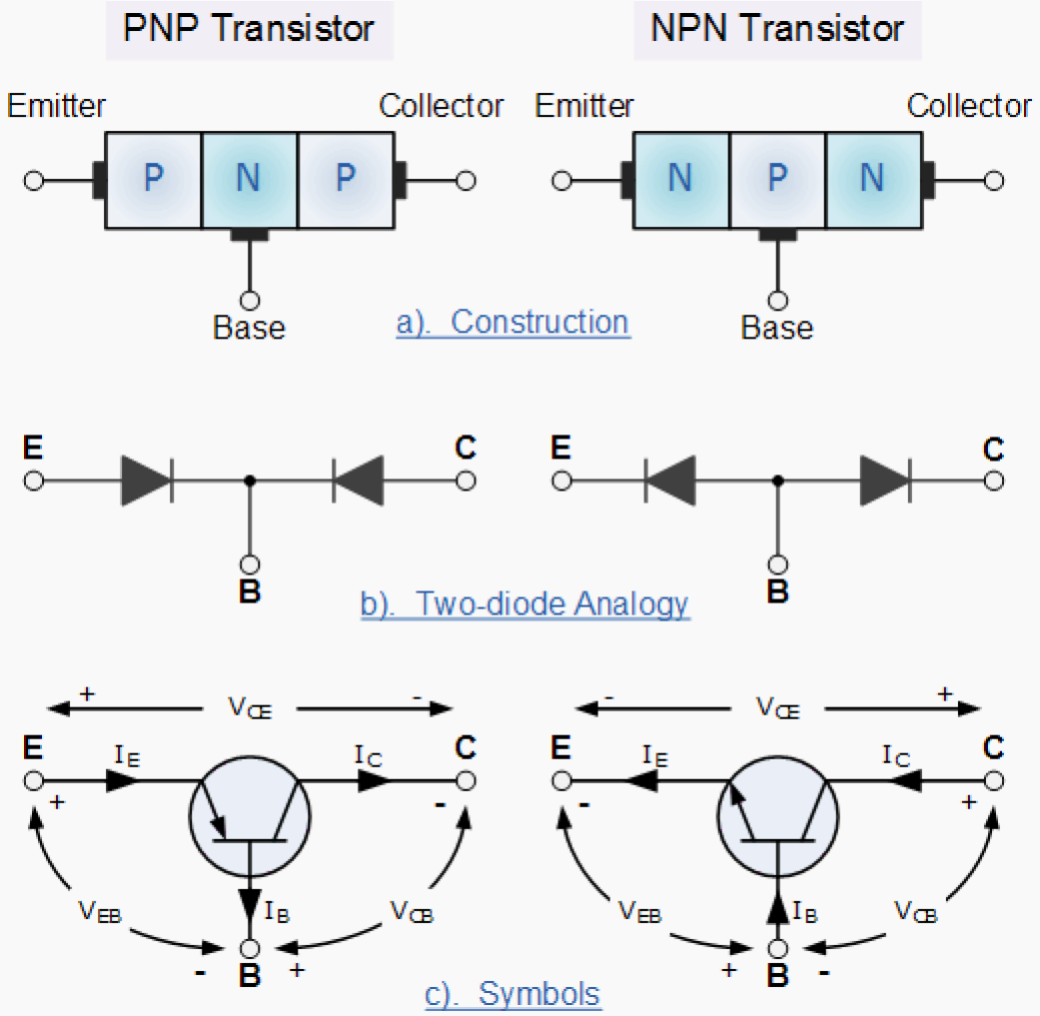


Fig Bipolar Junction Transistor Symbol

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

TRANSISTOR CURRENT COMPONENTS:

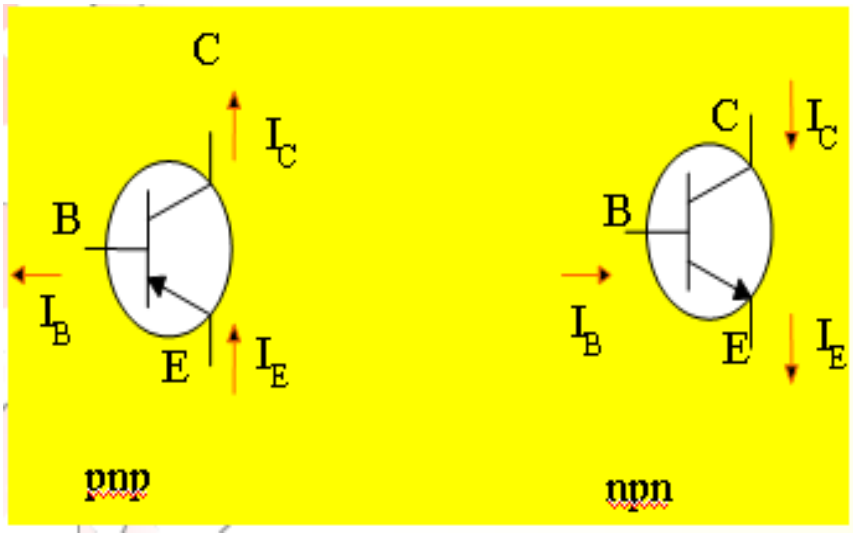


Fig Bipolar Junction Transistor Current Components

The above fig 3.2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{PE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter).The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter do not contribute carriers, which can reach the collector.

Not all the holes crossing the emitter junction J_E reach the the collector junction J_C

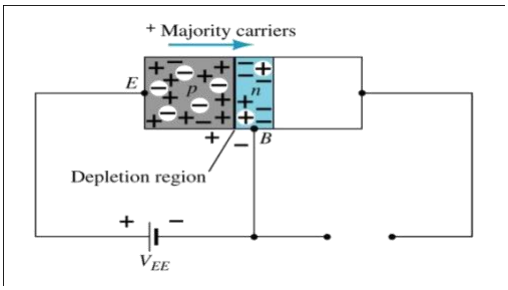
Because some of them combine with the electrons in n-type base. If I_{pC} is hole current at junction J_C there must be a bulk recombination current (I_{PE}- I_{pC}) leaving the base.

Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across $J_{E.}$ If the emitter were open circuited so that $I_E=0$ then I_{pC} would be zero. Under these circumstances, the base and collector current I_C would equal the reverse saturation current $I_{CO.}$ If $I_E \neq 0$ then

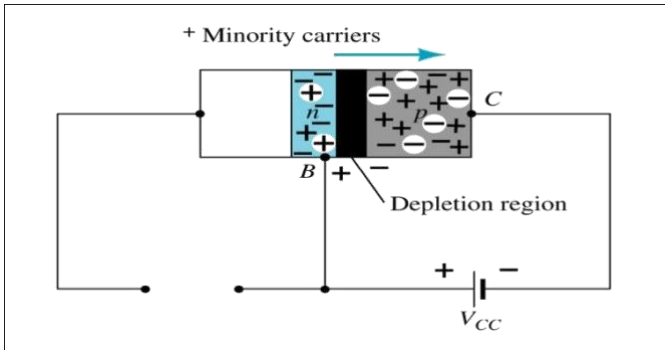
$I_C = I_{CO} - I_{pC}$

For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left, then for a p-n-p transistor, $I_{CO\ is}$ negative. For an n-p-n transistor, I_{CO} is positive.The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

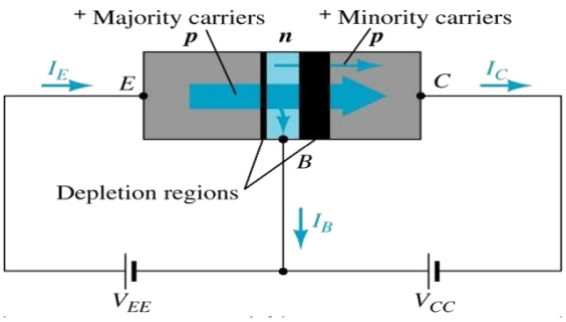
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



a Forward-biased junction of a pnp transistor



b Reverse-biased junction of a pnp transistor



c Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{Cmajority} + I_{COminority}$$

$I_{CO} – I_C$ current with emitter terminal open and is called leakage current Various parameters which relate the current components is given below **Emitter efficiency:**

$$\gamma = \frac{currentofinjectedcar riersatJ_E}{totalemitt ercurrent}$$

$$\gamma = \frac{I_{PE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\square^{*}\square\frac{injectedca\ rriercurrentreachingJ_C}{injectedca\ rrierncurrentatJ_E}$$

$$\square^{*}\square\frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off)to I_E the large signal current gain of a common base transistor.

$$\square\ \square\frac{\square\ (I_C\square\ I_{CO})}{I_E}$$

Since I_C and I_E have opposite signs, then α, as defined, is always positive. Typically numerical values of α lies in the range of 0.90 to 0.995

$$\square\ \square\frac{I_{pC}}{I_E}\square\frac{I_{pC}}{I_{nE}}*\frac{I_{pE}}{I_E}\quad\square\square\square*\square$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio $\square^{*}$ is unity. $\square^{*}$ is the ratio of total current crossing J_C to hole arriving at the junction.

Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and output of t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

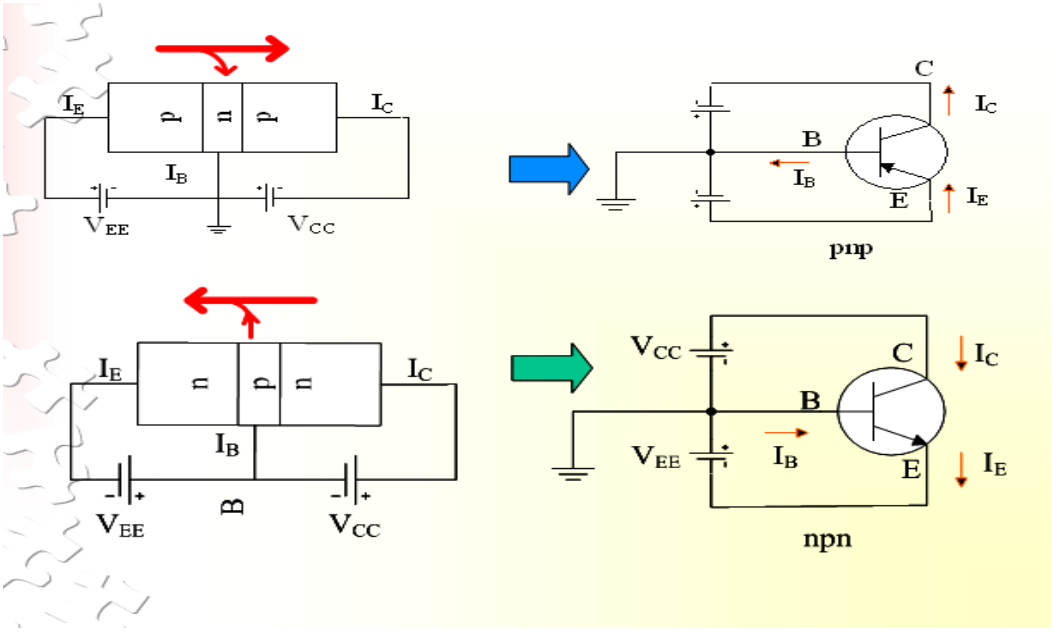


Fig CB Configuration

To describe the behavior of common-base amplifiers requires two set of characteristics:

1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A

- Saturation region- region of the characteristics to the left of $V_{CB} = 0V$

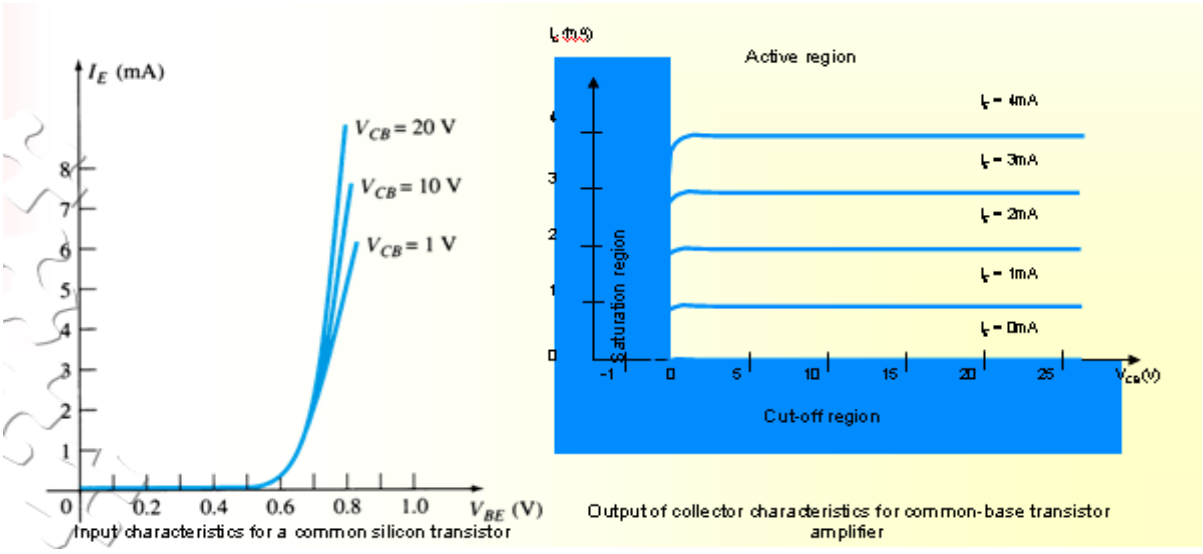


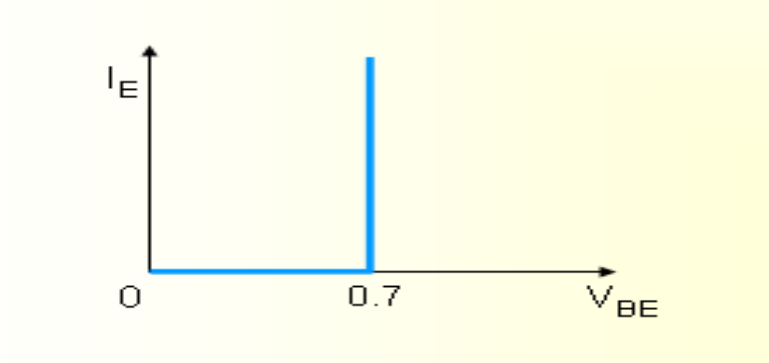
Fig CB Input-Output Characteristics

Active region	Saturation region	Cut-off region
•IE increased, Ic increased •BE junction forward bias and CB junction reverse bias •Refer to the graf, Ic ≈ IE •Ic not depends on VCB •Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in VCB will cause big different to Ic • The allocation for this region is to the left of VCB= 0 V.	• Region below the line of IE=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by

$I_C \approx IE$

Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be$V_{BE} = 0.7V$



In the dc mode the level of I_C and I_E due to the majority carriers are related by a quantity called alpha

$\square = \alpha_{dc}$

$I_C = \square I_E + I_{CBO}$

It can then be summarize to $I_C = \square I_E$ (ignore I_{CBO} due to small value)

For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by

α_{ac}

Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of $\square$ is typical from 0.9 ~ 0.998.

Biasing: Proper biasing CB configuration in active region by approximation $I_C \square I_E$ ($I_B \square$ 0 uA)

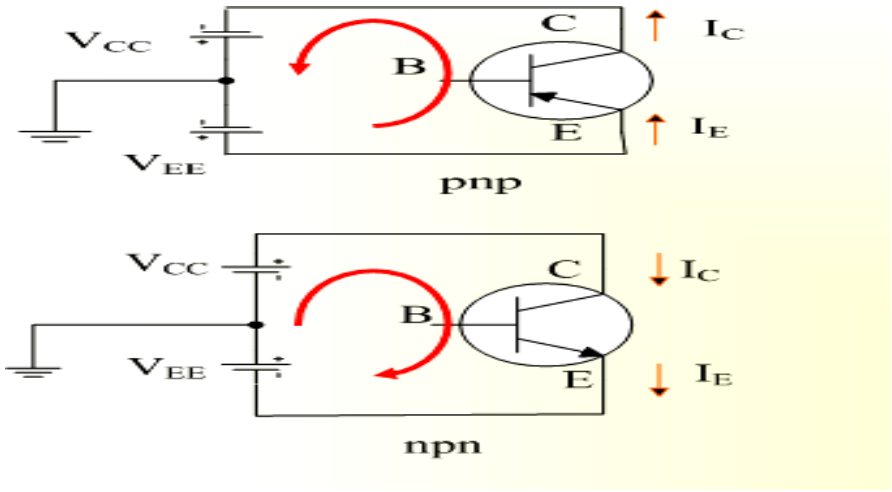


Fig CE Configuration

TRANSISTOR AS AN AMPLIFIER

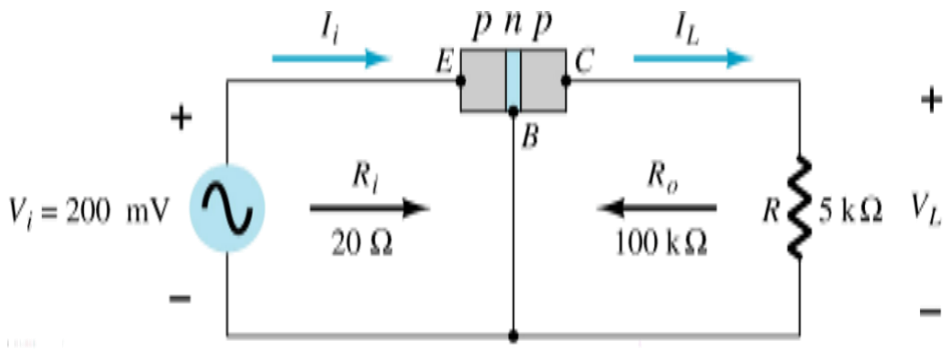


Fig Basic Transistor Amplifier Circuit

Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals.emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

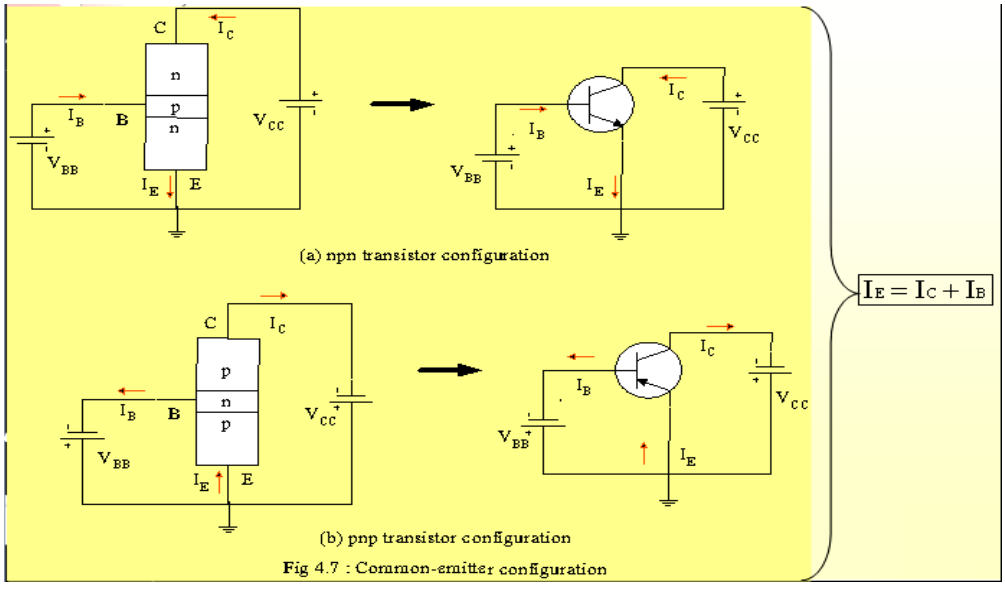


Fig 4.7 : Common-emitter configuration

Fig CE Configuration

I_B is microamperes compared to miliamperes of I_C.

I_B will flow when V_{BE} > 0.7V for silicon and 0.3V for germanium Before this value I_B is very small and no I_B.

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.

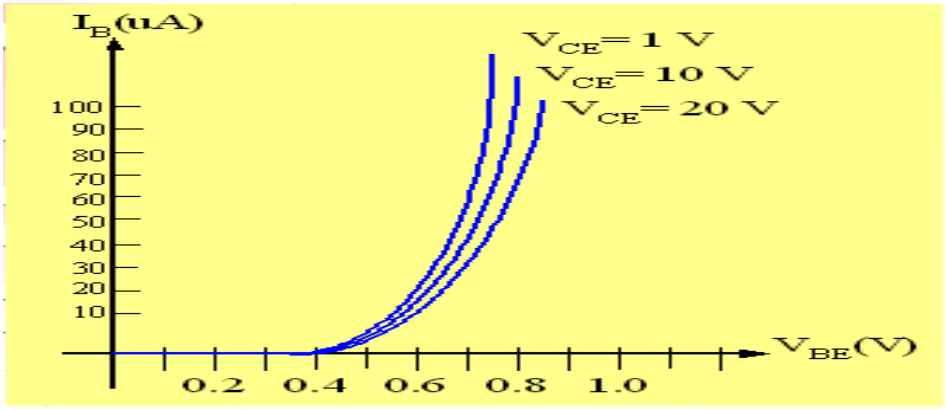


Fig a Input characteristics for common-emitter npn transistor

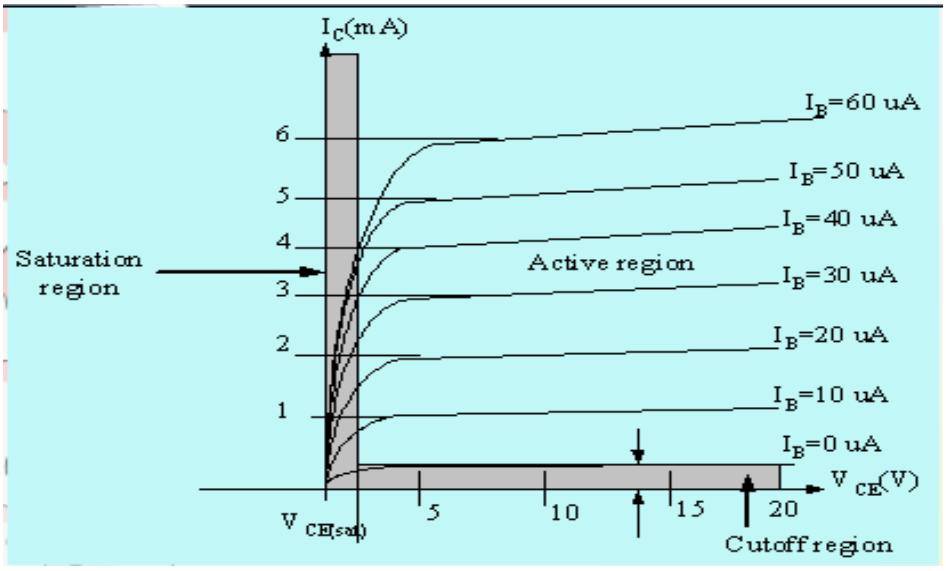


Fig b Output characteristics for common-emitter npn transistor

For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of

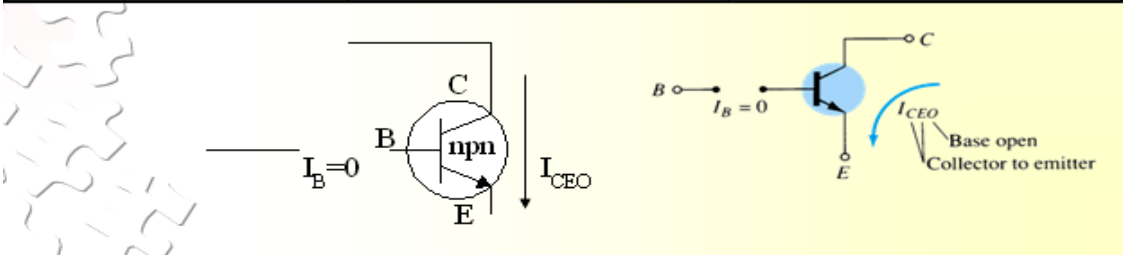
V_{CE} $V_{CE} > V_{CESAT}$ I_C not totally depends on V_{CE} □ constant I_C

I_B(uA) is very small compare to I_C (mA). Small increase in I_B cause big increase in

I_C I_B=0 A □ I_{CEO} occur.

Noticing the value when I_C=0A. There is still some value of current flows.

Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below I_B=0μA is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • I_B=0, I_C not zero, during this condition I_C=I_{CEO} where is this current flow when B-E is reverse bias.

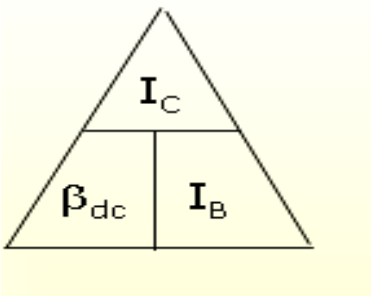


Beta (□) or amplification factor

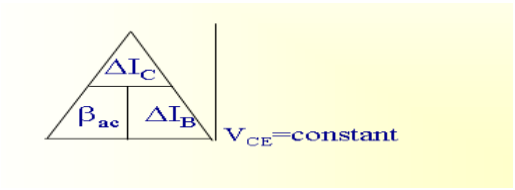
The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (□dc) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$$30 < \square_{dc} < 300 \quad \square \text{ 2N3904}$$

On data sheet, $\square_{dc}$=*hfe* with *h* is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.



For ac conditions, an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point. On data sheet, $\square_{ac}$=*hfe* It can defined by the following equation:



From output characteristics of commonemitter configuration, find $\square_{ac}$ and $\square_{dc}$ with an

Operating point at I_B=25 □A and V_{CE} =7.5V

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{ce}\ =\ \text{constant}}$$

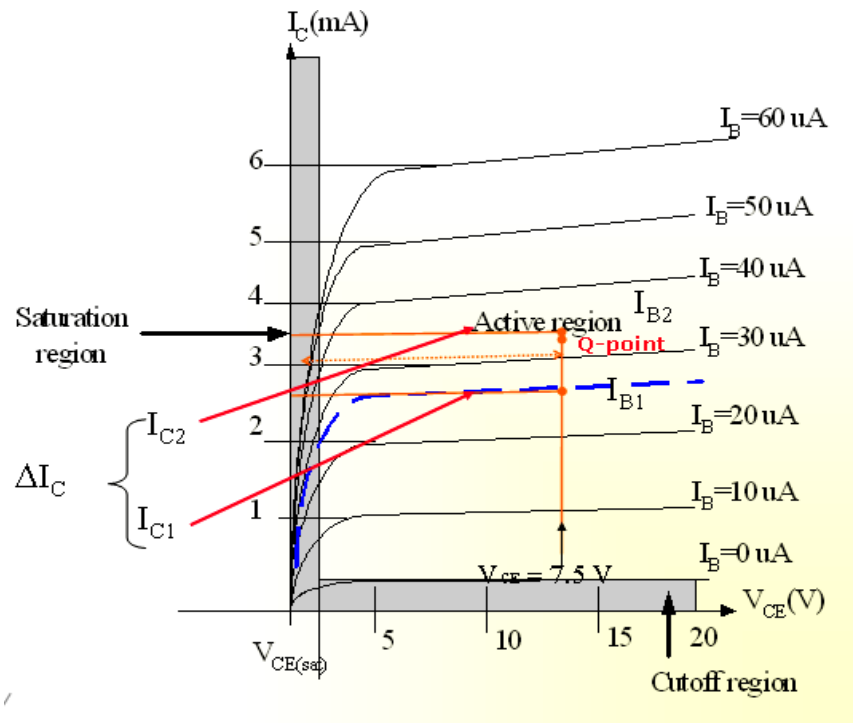
$$= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2\,\text{m} - 2.2\,\text{m}}{30\,\mu - 20\,\mu}$$

$$= \frac{1\,\text{m}}{10\,\mu} = 100$$

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$= \frac{2.7\,\text{m}}{25\,\mu}$$

$$= 108$$



Relationship analysis between α and β

CASE 1

$I_E = I_C + I_B$ (1)

subtitute equ. $I_C = \beta I_B$ into (1) we get

$$\underline{\underline{I_E = (\beta + 1) I_B}}$$

CASE 2

known : $\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$ (2)

known : $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$ (3)

subtitute (2) and (3) into (1) we get,

$$\underline{\underline{\alpha = \frac{\beta}{\beta + 1}}} \quad \text{and} \quad \underline{\underline{\beta = \frac{\alpha}{1 - \alpha}}}$$

COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point.The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is

similar with common-emitter. configuration.Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.

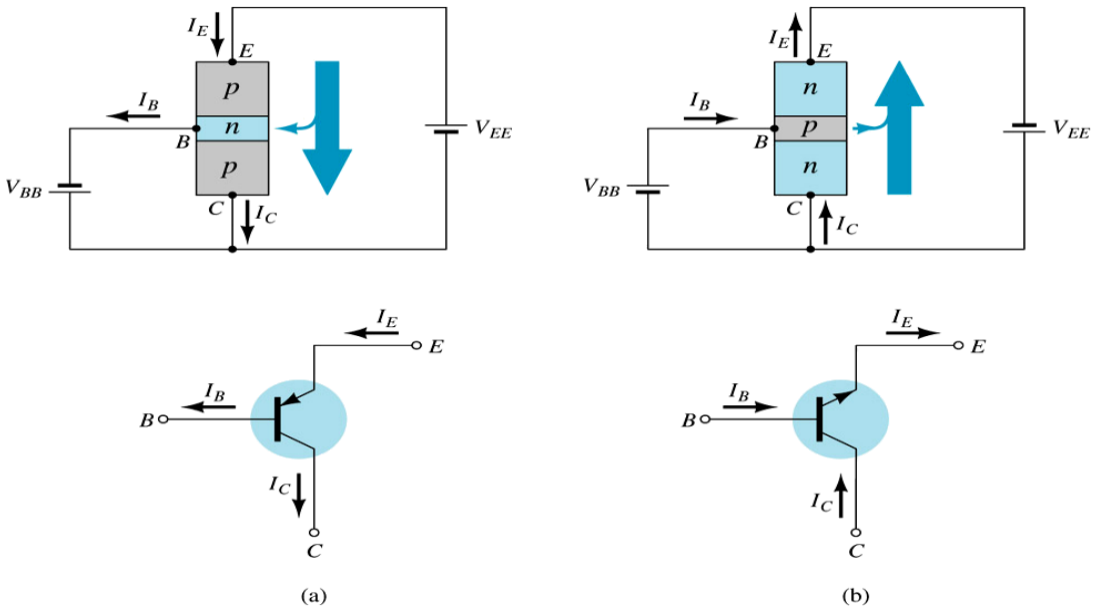


Fig CC Configuration

For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B.

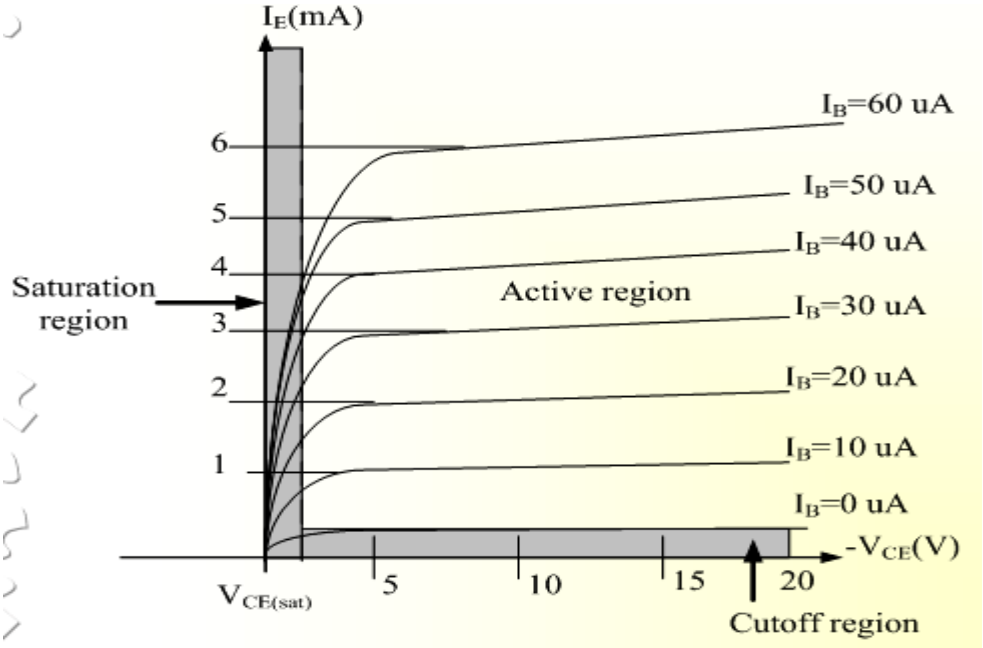


Fig Output Characteristics of CC Configuration for npn Transistor

Limits of opearation

Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations.At least 3 maximum values is mentioned in data sheet.

There are:

a) Maximum power dissipation at collector: P_{Cmax} or P_D

b) Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$) or V_{CEO}.

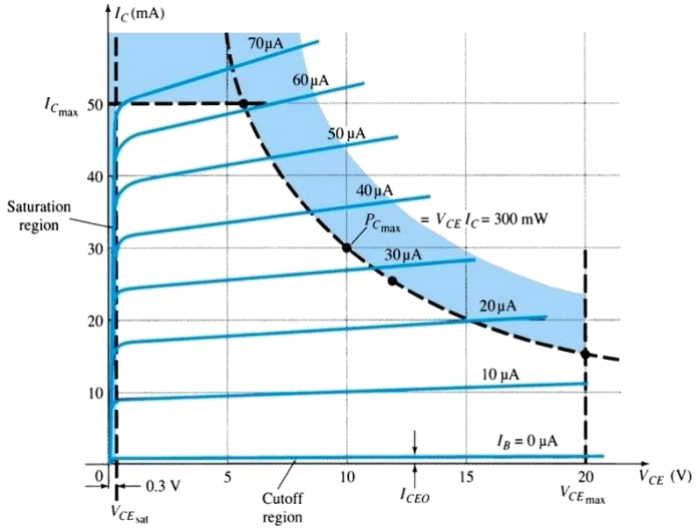
c) Maximum collector current: ICmax

There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are: transistor need to be operate in active region!

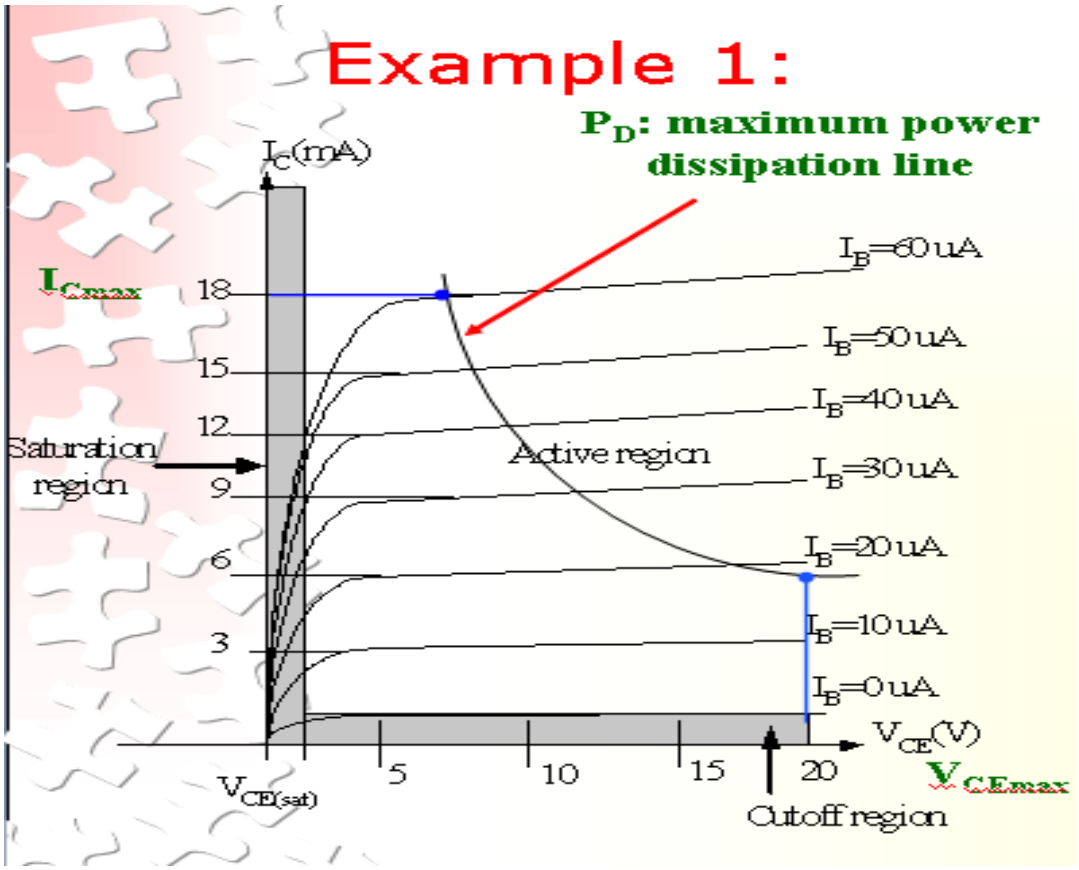
$I_C < I_{Cmax}$

P_C <

P_{Cmax}



Note: V_{CE} is at maximum and I_C is at minimum (I_{CMAX}=I_{CEO}) in the cutoff region. I_C is at maximum and V_{CE} is at minimum (V_{CE} max = V_{cesat} = V_{CEO}) in the saturation region. The transistor operates in the active region between saturation and cutoff.



Refer to the fig. Example; A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Step1:

The maximum collector power dissipation,

P_D=I_{CMAX} x V_{CEmax}= 18m x 20 = 360 mW

Step 2:

At any point on the characteristics the product of and must be equal to 360 mW. Ex.

1. If choose I_{Cmax}= 5 mA, substitute into the (1), we get

$V_{CEmax}I_{Cmax}$= 360 mW

V_{CEmax}(5 m)=360/5=7.2

V

Ex.2. If choose V_{CEmax}=18 V, substitute into (1), we get

$V_{CEmax}I_{Cmax}$= 360 mW

(10) I_{CMAX}=360m/18=<u>20 mA</u>

Derating P_{Dmax}

P_{DMAX} is usually specified at 25°C.

The higher temperature goes, the less is P_{DMAX}

Example;A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

NEED FOR TRANSISTOR BIASING

Operating Point

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1) Emitter base junction must be forward biased (V_{BE}=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
2) V_{ce} voltage should not fall below $V_{CE\ (sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE\ (sat)}$ the collector base junction is not probably reverse biased.
3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current t due to signal alone.
4) Max. rating of the transistor $I_{c(max)}$, $V_{CE\ (max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, I_c=0, V_{CE} =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

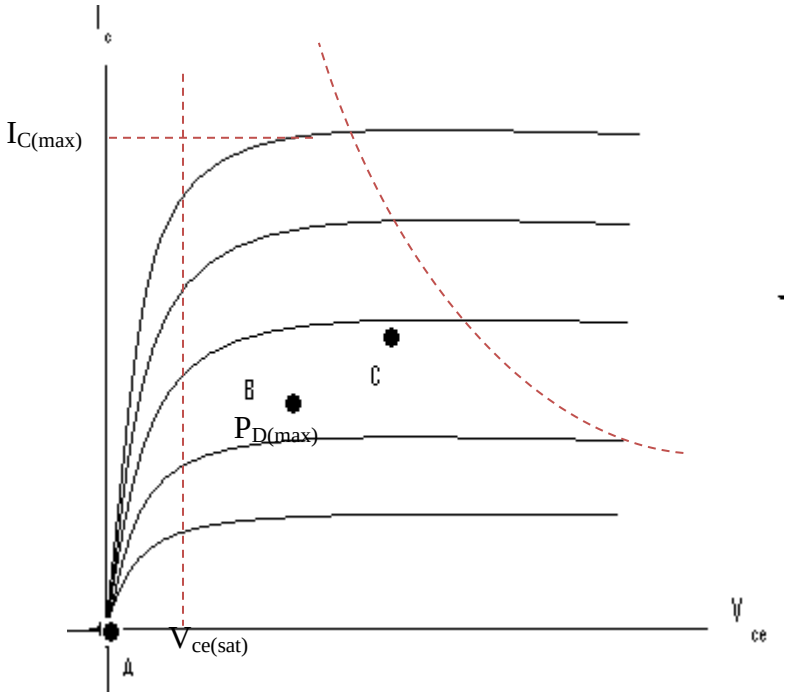


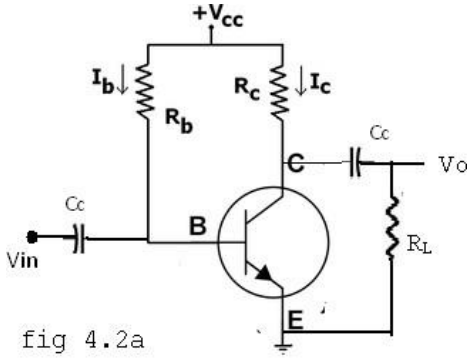
Fig 4.1CE Output Characteristics

4.2 DC LOAD LINE

Referring to the biasing circuit of fig 4.2a, the values of V_{CC} and R_C are fixed and Ic and V_{CE} are dependent on R_B.

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$Vcc = IcRc + Vce$$



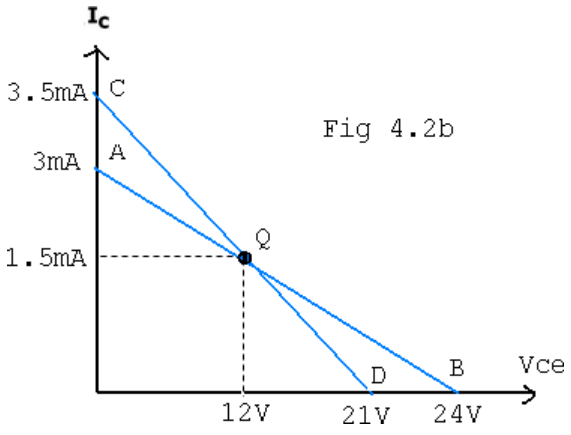


Fig 4.2b

Fig 4.2a CE Amplifier circuit (b) Load line

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting V_{CE} =0 in the above equation. Then $Ic = \frac{Vcc}{Rc}$. Therefore The coordinates of A are V_{CE} =0 and $Ic = \frac{Vcc}{Rc}$.

The coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are V_{CE} =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10°C raise in temperature
2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per °C
3) Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given I_B. Hence , in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

4.3 AC LOAD LINE

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance R_{ac}, is a combination of R_C parallel to R_L i.e. $R_{ac} = R_L \| R_C$. So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, I.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

$V_{CE(max)} = V_{CEQ} + I_{CQ}R_{ac}$, which locates point D on the Vce axis.

$I_{c(max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the I_C axis.

By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than ac load line.

4.4 STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

1) VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

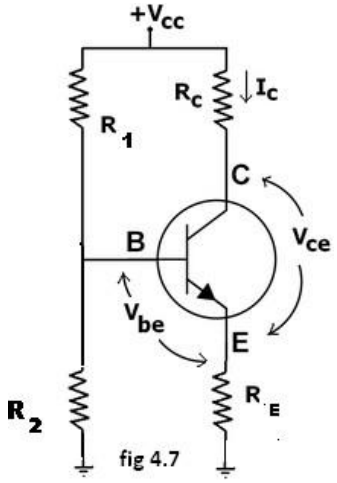


Fig 4.7 Voltage Divider Biasing Circuit

In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{ provided } I_B << I_2 = V_B/R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1+R_2}$$

$$V_2 = \frac{V_{CC}}{R_1+R_2}\cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$
$$V_2 = V_{BE} + I_E R_E$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$
$$I_E = \frac{V_2 - V_{BE}}{R_E}$$
$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$\because I_C \cong I_E$$
$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq} + R_E)}{R_{eq} + R_E(1+\beta)}$$
$$R_{eq} = R_1 || R_2$$
$$S = \frac{(1+\beta)\left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \| R_2$ very low.

- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

- AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

4.5 THERMAL RUNAWAY AND THERMAL STABILITY

THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1+\beta)I_{CO}$. The three variables in the equation, β, I_B, and I_{CO} increases with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature. Specifically it doubles for every 10°C rise in temperature. The collector current I_C causes the collector base junction temperature to rise which in turn, increase I_{CO}, as a result I_C will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to

"thermal runaway". Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the $(1+\beta)I_{CO}$, keeping I_C almost constant.

THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is $T_A{}^oC$ and the temperature of the collector-base junction of the transistor is $T\ ^oC$.

Due to heating within the transistor T_J is higher than T_A. As the temperature difference T_J- T_A is greater, the power dissipated in the transistor, P_D will be greater, i.e, T_J- T_A P_D

The equation can be written as = T_J- T_A P_D. , where is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation = T_J- T_A /P_D. Hence is measured in $^oC/W$ which may be as small as 0.2 $^oC/W$ for a high power transistor that has an efficient heat sink or up to $1000^oC/W$ for small signal, low power transistor which have no cooling provision.

As Θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as Θ_{J-A}. However, for power transistors, thermal resistance is given form junction to case, Θ_{J-C}.

The amount resistance from junction to ambience is considered to consist of 2 parts.

$\Theta_{J-A} = \Theta_{J-C} - \Theta_{C-A}$.

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence the power dissipated.

$P_D = (T_J - T_A)/\Theta_{J-A}$

$=(T_J - T_A)/(\Theta_{J-C} + \Theta_{C-A})$

Θ_{J-C} is determined by the type of manufacture of the transistor and how it is located I the case, but Θ_{C-A} is determined by the surface area of the case or flange and its contact with air. If the effective surface area of the transistor case could be increased, the resistance to heat flows, or could be increased Θ_{C-A}, could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance Θ_{HS-A}.

This thermal resistance is not added to Θ_{C-A} in series, but is instead in parallel with it and if

Θ_{HS-A} is much less than Θ_{C-A}, then Θ_{C-A} will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} || \Theta_{HS-A}$.

4.6 CONDITION FOR THERMAL STABILITY

For preventing thermal runaway, the required condition I the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$$P_C = I_C V_{CB} \approx I_C V_{CE}$$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$P_C = I_C V_{CC} - I_C^2(R_E + R_C)$.....(1)

The condition to prevent thermal runaway can be written as

$$\frac{\partial P_C}{\partial I_C}\frac{\partial I_C}{\partial T_j} < \frac{1}{\Theta} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

As$\Theta$and $\frac{\partial I_C}{\partial T_j}$ are positive, $\frac{\partial P_C}{\partial I_C}$ should be negative in order to satisfy the above condition. Differentiating equation (1) w.r.t I_C we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C(R_E + R_C) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Hence to avoid thermal runaway it is necessary that

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Emitter Follower

Emitter follower circuit has a prominent place in feedback amplifiers. Emitter follower is a case of negative current feedback circuit. This is mostly used as a last stage amplifier in signal generator circuits.

The important features of Emitter Follower are −

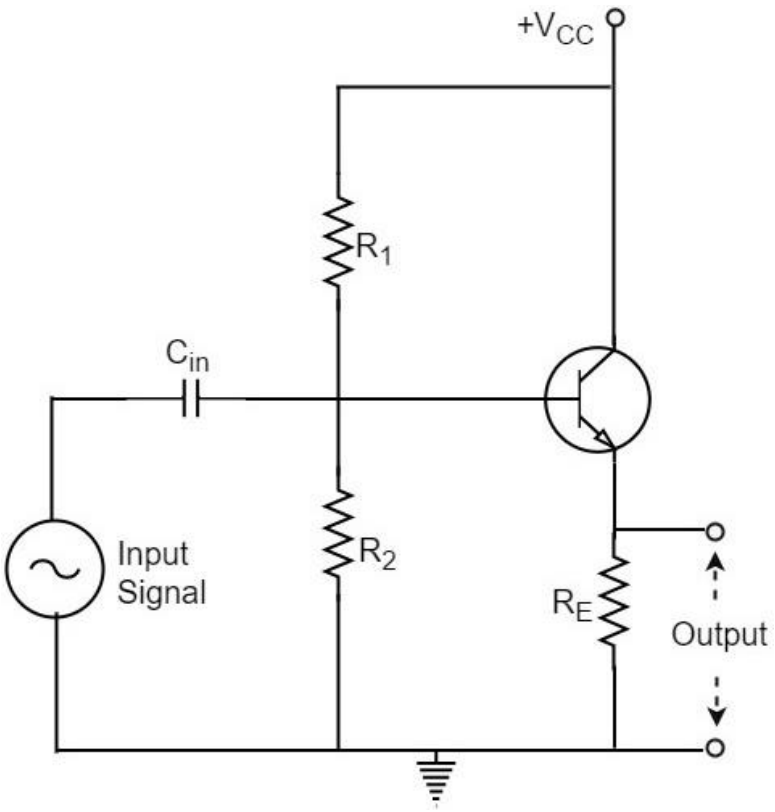
- It has high input impedance
- It has low output impedance
- It is ideal circuit for impedance matching

All these ideal features allow many applications for the emitter follower circuit. This is a current amplifier circuit that has no voltage gain.

Construction

The constructional details of an emitter follower circuit are nearly similar to a normal amplifier. The main difference is that the load R_L is absent at the collector terminal, but present at the emitter terminal of the circuit. Thus the output is taken from the emitter terminal instead of collector terminal.

The biasing is provided either by base resistor method or by potential divider method. The following figure shows the circuit diagram of an Emitter Follower.



Operation

The input signal voltage applied between base and emitter, develops an output voltage V_o across R_E, which is in the emitter section. Therefore,

$$V_o = I_E R_E V_o = I_E R_E$$

The whole of this output current is applied to the input through feedback. Hence,

$$V_f = V_o V_f = V_o$$

As the output voltage developed across R_L is proportional to the emitter current, this emitter follower circuit is a current feedback circuit. Hence,

$$\beta = \frac{V_f}{V_o} = 1 \beta = \frac{V_f}{V_o} = 1$$

It is also noted that the input signal voltage to the transistor (= V_i) is equal to the difference of V_s and V_o i.e.,

$$V_i = V_s - V_o V_i = V_s - V_o$$

Hence the feedback is negative.

Characteristics

The major characteristics of the emitter follower are as follows −

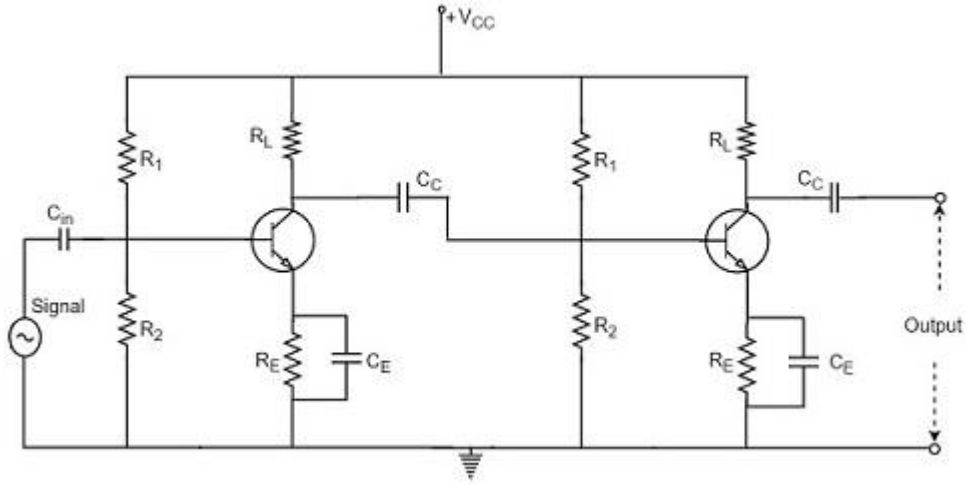
- No voltage gain. In fact, the voltage gain is nearly 1.
- Relatively high current gain and power gain.
- High input impedance and low output impedance.

- Input and output ac voltages are in phase.

RC Coupled Amplifier

The constructional details of a two-stage RC coupled transistor amplifier circuit are as follows. The two stage amplifier circuit has two transistors, connected in CE configuration and a common power supply V_{CC} is used. The potential divider network R_1 and R_2 and the resistor R_e form the biasing and stabilization network. The emitter by-pass capacitor C_e offers a low reactance path to the signal.

The resistor R_L is used as a load impedance. The input capacitor C_{in} present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor C_C is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point. The figure below shows the circuit diagram of RC coupled amplifier.



Operation of RC Coupled Amplifier

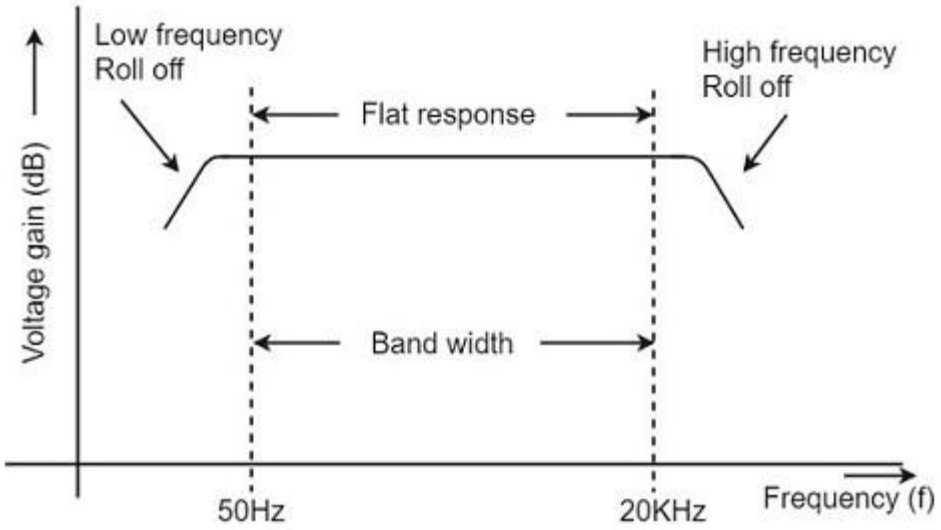
When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load R_L which is then passed through the coupling capacitor C_C to the next stage. This becomes the input of the next stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages. This is because when a second stage is made to follow the first stage, the **effective load resistance** of the first stage is reduced due to the shunting effect of the input resistance of the second stage. Hence, in a multistage amplifier, only the gain of the last stage remains unchanged.

As we consider a two stage amplifier here, the output phase is same as input. Because the phase reversal is done two times by the two stage CE configured amplifier circuit.

Frequency Response of RC Coupled Amplifier

Frequency response curve is a graph that indicates the relationship between voltage gain and function of frequency. The frequency response of a RC coupled amplifier is as shown in the following graph.



From the above graph, it is understood that the frequency rolls off or decreases for the frequencies below 50Hz and for the frequencies above 20 KHz. whereas the voltage gain for the range of frequencies between 50Hz and 20 KHz is constant.

We know that,

$XC=12\pi fcXC=12\pi fc$

It means that the capacitive reactance is inversely proportional to the frequency.

At Low frequencies (i.e. below 50 Hz)

The capacitive reactance is inversely proportional to the frequency. At low frequencies, the reactance is quite high. The reactance of input capacitor C_{in} and the coupling capacitor C_C are so high that only small part of the input signal is allowed. The reactance of the emitter by pass capacitor C_E is also very high during low frequencies. Hence it cannot shunt the emitter resistance effectively. With all these factors, the voltage gain rolls off at low frequencies.

At High frequencies (i.e. above 20 KHz)

Again considering the same point, we know that the capacitive reactance is low at high frequencies. So, a capacitor behaves as a short circuit, at high frequencies. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Along with this, as the capacitance of emitter diode decreases, it increases the base current of the transistor due to which the current gain (β) reduces. Hence the voltage gain rolls off at high frequencies.

At Mid-frequencies (i.e. 50 Hz to 20 KHz)

The voltage gain of the capacitors is maintained constant in this range of frequencies, as shown in figure. If the frequency increases, the reactance of the capacitor C_C decreases which tends to

increase the gain. But this lower capacitance reactive increases the loading effect of the next stage by which there is a reduction in gain.

Due to these two factors, the gain is maintained constant.

Advantages of RC Coupled Amplifier

The following are the advantages of RC coupled amplifier.

- The frequency response of RC amplifier provides constant gain over a wide frequency range, hence most suitable for audio applications.
- The circuit is simple and has lower cost because it employs resistors and capacitors which are cheap.
- It becomes more compact with the upgrading technology.

Disadvantages of RC Coupled Amplifier

The following are the disadvantages of RC coupled amplifier.

- The voltage and power gain are low because of the effective load resistance.
- They become noisy with age.
- Due to poor impedance matching, power transfer will be low.

Applications of RC Coupled Amplifier

The following are the applications of RC coupled amplifier.

- They have excellent audio fidelity over a wide range of frequency.
- Widely used as Voltage amplifiers
- Due to poor impedance matching, RC coupling is rarely used in the final stages.

Cascading of Amplifier Stages

A single stage of amplifier can provide only a limited current gain or voltage gain. Most of the applications require much higher gain. Hence, we usually use several amplifier stages connected in cascade i.e. connected such that the output of one stage becomes the input to the next stage. Thus, a multistage amplifier or cascade amplifier may provide a higher voltage gain or current gain.

Cascading of amplifier stages is usually done to increase the total gain of the amplifier. However, sometimes cascading is done to get the desired output and input impedance for specific applications. Figure 1 gives the block diagram of two-stage amplifier. The first stage is driven by a voltage source V_s having series source resistance R_s. Alternatively, the driving source may be current source I_s with shunt resistance R_s. the output of the first stage is fed to the input of the second stage while the output of the second stage feeds the load impedance Z_L.

Actual voltage available at the input of the first stage is V_i while V_0 is the output voltage of the second stage. Then the ratio $\frac{V_o}{V_i}$ forms the voltage gain of the two stage cascade amplifier. Instead of two stages as shown in figure 3, we may have three or more stages connected in cascade

amplifier, it becomes possible to amplify a weak input voltage V_i of just a few microvolts to get an output voltage V_0 of several volts.

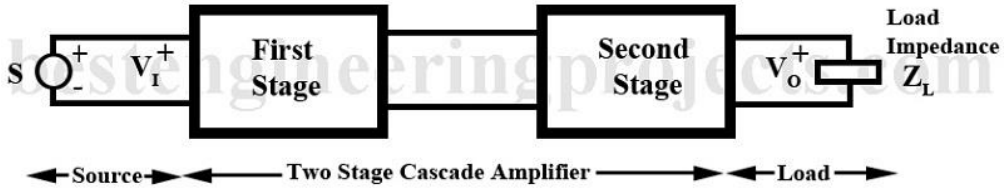


Figure 1:- Block Diagram of Two Stage Cascade Amplifiier

Cascading of Amplifier Stage using Transistor

Transistor amplifier may be connected in any of the three configurations namely common emitter (CE), common base (CB) and common collector (CC). However, in cascade amplifier meant for providing high gain, only CE amplifier stage are connected in cascade. CB and CC configurations can not be used for this purpose.

Figure 2 gives the circuit of a two stage CE audio amplifier. The circuit gives the typical biasing arrangement and use of coupling capacitors C_{b1} and C_{b2}. Typical values of circuit components are also given. The load impedance is a resistor while coupling is through a capacitor. Hence this cascade amplifier forms the so-called resistance – Capacitance coupled or RC coupled amplifier. Other circuit arrangement is also popular for specific uses. However, we here take up R.C. coupled amplifier since this is the one most popularly used for audio frequency amplification. Circuit of figure 2 is given here just to give an impression as to what a typical 2-stage CE audio amplifier looks like.

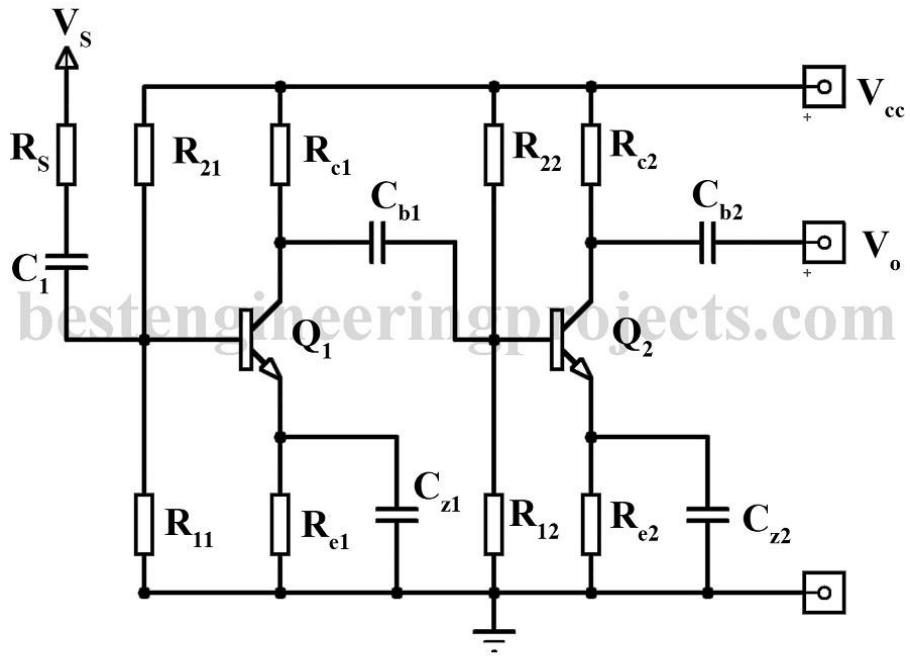


Figure 2:- Two-Stage CE Audio Amplifier

Analysis | Cascading of Amplifier Stages

For the purpose of analysis we take up a general n-stage CE cascade amplifier. Figure 3 gives the block diagram of the same giving the various voltages, currents and resistances involved. In Figure 3, the biasing

arrangement and coupling elements have not been shown for the sake of celerity. We now proceed to derive expressions for voltage gain, current gain, power gain, input impedance and output impedance of this amplifier.

(A) Voltage Gain:

The voltage gain of the complete cascade amplifier is simply the product of the voltage gains of the individual stage. This is proved below.

Voltage gain of first stage is,

$$A_{V1} = \frac{V_2}{V_1} = \frac{Output\ voltage\ of\ the\ first\ stage}{Input\ voltage\ of\ the\ first\ stage}$$
$$= A_{V1} < \theta_1 \quad \text{.....(1)}$$

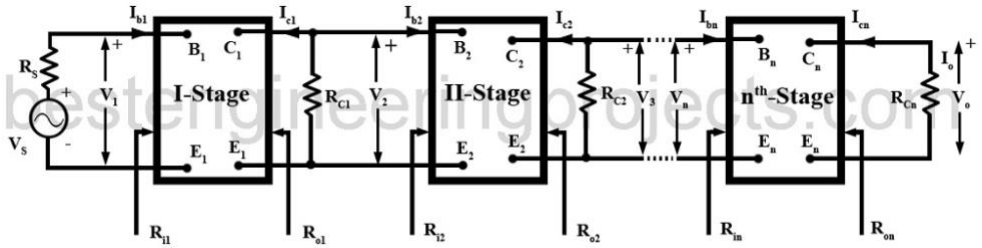


Figure 3: n-Stage CE Cascade Amplifier

Where A_{V1} is the magnitude of the voltage gain and θ_1 is the phase angle of the output voltage V_2 relative to the input voltage V_1. The output voltage V_2 of the first stage forms the input voltage of the second stage. Hence

Voltage gain of second stage is,

$$A_{V2} = \frac{V_3}{V_2} = \frac{Output\ voltage\ of\ the\ second\ stage}{Input\ voltage\ of\ the\ first\ stage}$$
$$= A_{V2} < \theta_2 \quad \text{……(2)}$$

Similar expressions may be written for the remaining stages.

Then the voltage gain of the complete n-stage cascade amplifier is given by,

$$A_V = \frac{V_0}{V_1} = \frac{Output\ voltage\ of\ the\ n^{th}\ stage}{Input\ voltage\ of\ the\ first\ stage}$$
$$= A_V < \theta \quad \text{.....(3)}$$

Where A_v is the magnitude of the voltage gain and θ is the phase angle of the output voltage V_0 relative to the input voltage V_1

But ……(4)

From equation 4 we conclude that

$$A_V = A_{V1} \times A_{V2} \times A_{V3} \ldots . A_{Vn-1} \times A_{Vn} \quad \text{……(5)}$$

Or $A_V < \theta = A_{V1} \times A_{V2} \times A_{V3} \ldots . A_{Vn-1} \times A_{Vn}$

$=< \theta_1 + \theta_2 + \ . \ . \ . \ . + \theta_n$ …..(6)

Hence $A_V = A_{V1} \times A_{V2} \times A_{V3} \ . \ . \ . \ . A_{V2}$ ……(7)

And $\theta = \theta_1 + \theta_2 + \theta_3 + \ . \ . \ . \ . + \theta_n$ ……(8)

From Equation (7) we conclude that the magnitude of voltage gain of the complete cascade amplifier is equal to the product of the magnitude of voltage gains of the individual stages.

From Equations 8 we conclude that the phase shift of the voltage gain of the complete cascade amplifier is equal to the sum of the phase shift of the individual stages.