UNIT-III

FETS & DIGITAL CIRCUITS

Basic Definitions:

The FET is a semiconductor device whose operation consists of controlling the flow of current through a semiconductor channel by application of an electric field (voltage)There are two categories of FETs: the junction field-effect transistor (JFET) and the metal-oxide-semiconductor field-effect transistor (MOSFET). The MOSFET category is further broken-down into: depletion and enhancement types.

A Comparison between FET and BJT:

- FET is a unipolar device. It operates as a voltage-controlled device with either electron current in an n-channel FET or hole current in a p-channel FET.
- BJT made as npn or as pnp is a current-controlled device in which both electron current and hole current are involved.
- The FET is smaller than a BJT and is thus for more popular in integrated circuits)ICs).
- FETs exhibit much higher input impedance than BJTs.
- FETs are more temperature stable than BJTs.
- BJTs have large voltage gain than FETs when operated as an amplifier.
- The BJT has a much higher sensitivity to changes in the applied signal (faster response) than a FET.

Junction Field-Effect Transistor (JFET(:

The basic construction of n-channel (p-channel) JFET is shown in Fig. 1-1a (b).Note that the major part of the structure is n-type (p-type) material that forms the channel between the embedded layers of p-type (n-type) material. The top of the n-type(p-type) channel is connected through an ohmic contact to a terminal referred to as the drain "D", while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source "S". The two p-type materials are connected together and to the gate "G" terminal.

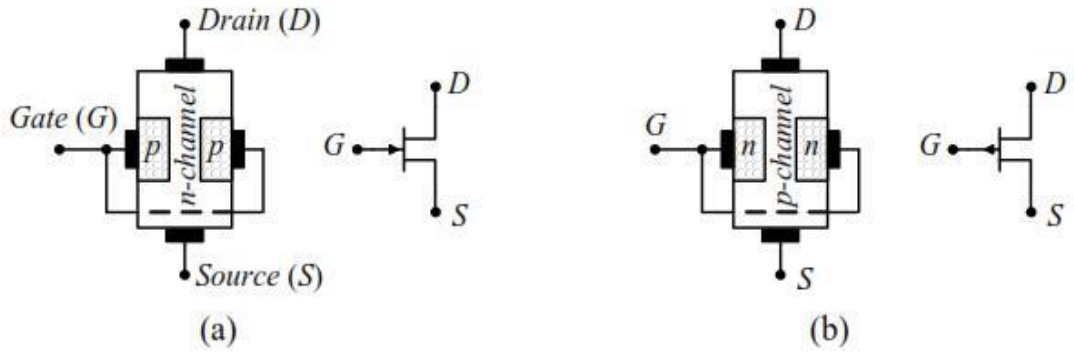


Fig. (1-1)

Basic Operation of JFET:

- Bias voltages are shown, in Fig. 1-2, applied to an n-channel JFET devise.
- VDD provides a drain-to-source voltage, VDS, (drain is positive relative to source) and supplies current from drain to source, ID, (electrons move from source to drain(.
- VGG sets the reverse-bias voltage between the gate and the source, VGS, (gate is biased negative relative to the source).
- Input impedance at the gate is very high, thus the gate current IG = 0 A.

- Reverse biasing of the gate-source junction produces a depletion region in the n-channel and thus increases its resistance.

- The channel width can be controlled by varying the gate voltage, and thereby, ID can also be controlled.
- The depletion regions are wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.

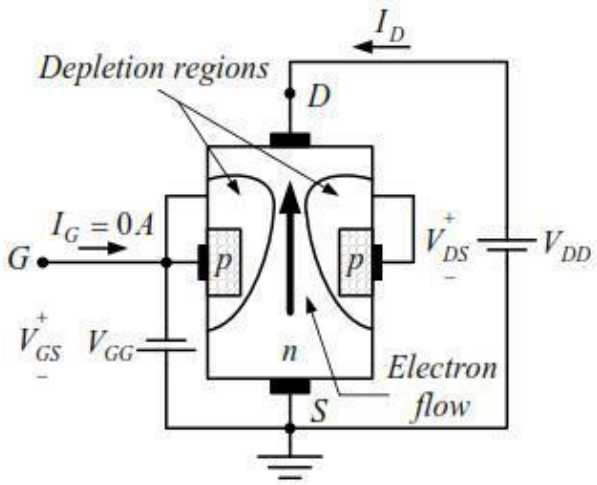


Fig. (1-2)

JFET Characteristics:

When VGS = 0 V and VDS < VP **(pinch-off voltage):** ID rises linearly with VDS **(ohmic region, n-channel resistance is constant)**, as shown in Fig. 1-3.

- When VDS is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of VDS that establishes this condition is referred to as the pinch-off voltage and is denoted by VP.

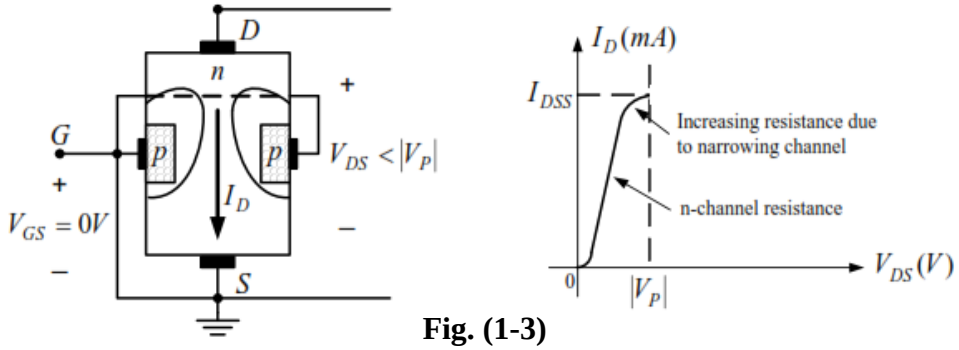


Fig. (1-3)

- When VGS = 0 V and VDS ≥ VP : ID remains at its saturation value IDSS beyond VP, as shown in Fig. 1-4.

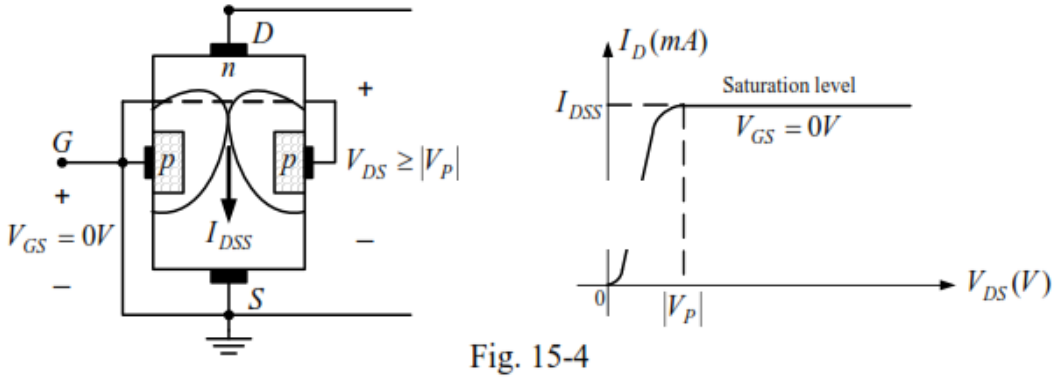


Fig. 15-4

When VGS < 0 and VDS some positive value: The effect of the applied negative-bias VGS is to establish depletion regions similar to those obtained with VGS = 0 V but at lower levels of VDS. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at lower level of VDS, as shown in Fig. 1-5.

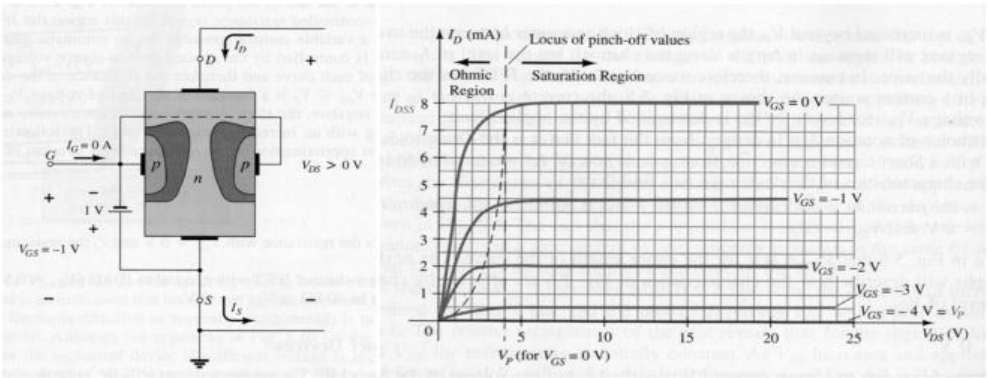


Fig. (1-5)

Summary:

- **For n-channel JFET:**

1. The maximum current is defined as IDSS and occurs when VGS = 0 V and VDS ≥ VP as shown in Fig. 1-6a.
2. For gate-to-source voltages VGS less than (more negative than) the pinch-off level, the drain current is 0 A (ID = 0 A) as appearing in Fig. 1-6b.
3. For all levels of VGS between current 0 V and the pinch-off level, the IDSS ID will range between shown in Fig. 1- and 0 A, respectively, as 6c.

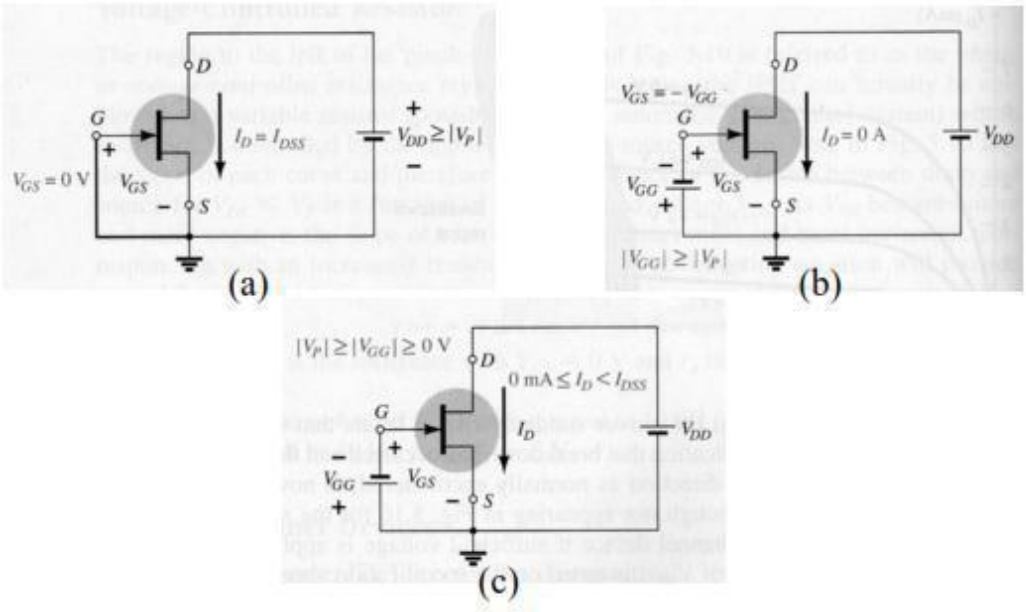


Fig. (1-6)

- **For p-channel JFET:**

a similar list can be developed (see Fig. 1-7(.

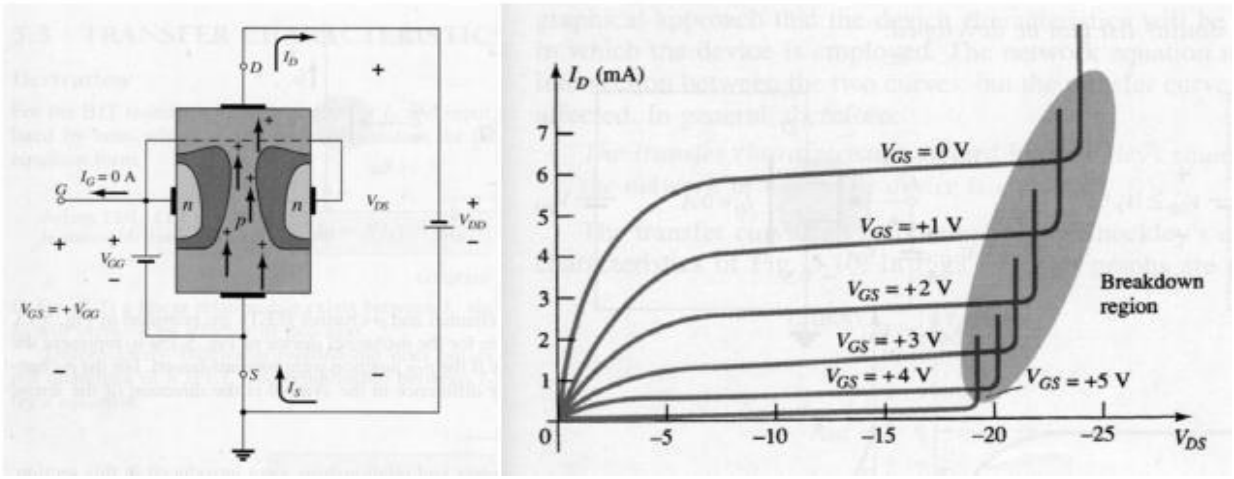


Fig.(1-7)

Shockley's Equation:

For the BJT the output current IC and input controlling current IB were related by β, which was considered constant for the analysis to be performed. In equation form:

control variable

$$I_C = \beta \cdot I_B$$

constant

In the above equation a linear relationship exists between IC and IB.

Unfortunately, this linear relationship does not exist between the output (ID) and input (VGS) quantities of a JFET. The relationship between ID and VGS is defined by Shockley's equation:

control variable

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

constant

[1.1]

The squared term of the equation will result in a nonlinear relationship between ID and VGS, producing a curve that grows exponentially with decreasing magnitude of VGS.

Transfer Characteristics:

Transfer characteristics are plots of ID versus VGS for a fixed value of VDS. The transfer curve can be obtained from the output characteristics as shown in Fig. 1-8, or it can be sketched to a satisfactory level of accuracy (see Fig. 1-9) simply using Shockley's equation with the four plot points defined in Table 1-1.

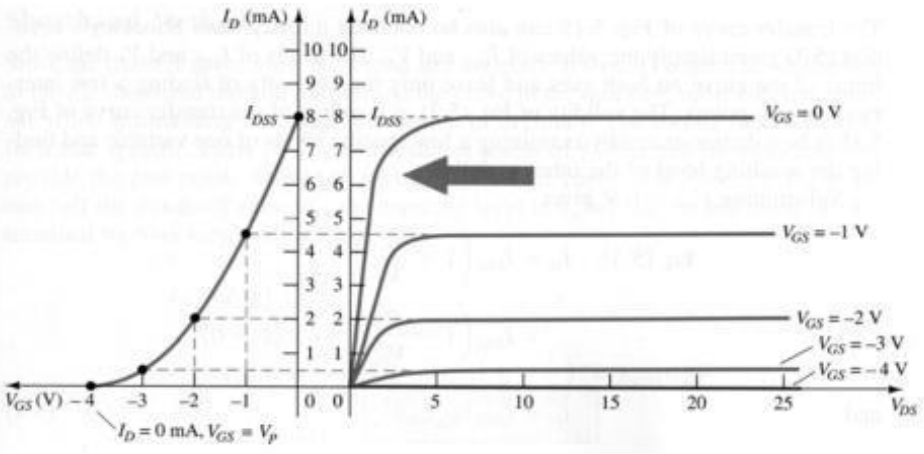


Fig.(1-8)

Table 1-1

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	
V_{GS} (V)	I_D (mA)
0	I_{DSS}
0.3 V_P	I_{DSS} / 2
0.5 V_P	I_{DSS} / 4
V_P	0

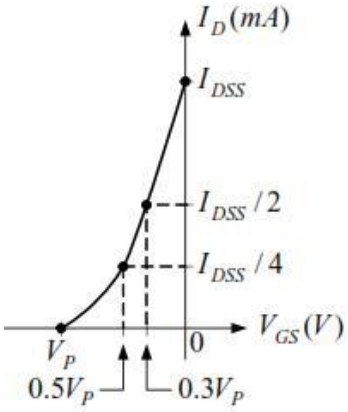


Fig.(1-9)

Important Relationships:

A number of important equations and operating characteristics have introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. In an effort to isolate and emphasize their importance, they are repeated below next to a corresponding equation for the BJT. The JFET equations are defined for the configuration of Fig. 1-10a, while the BJT equations relate to Fig. 1-10b.

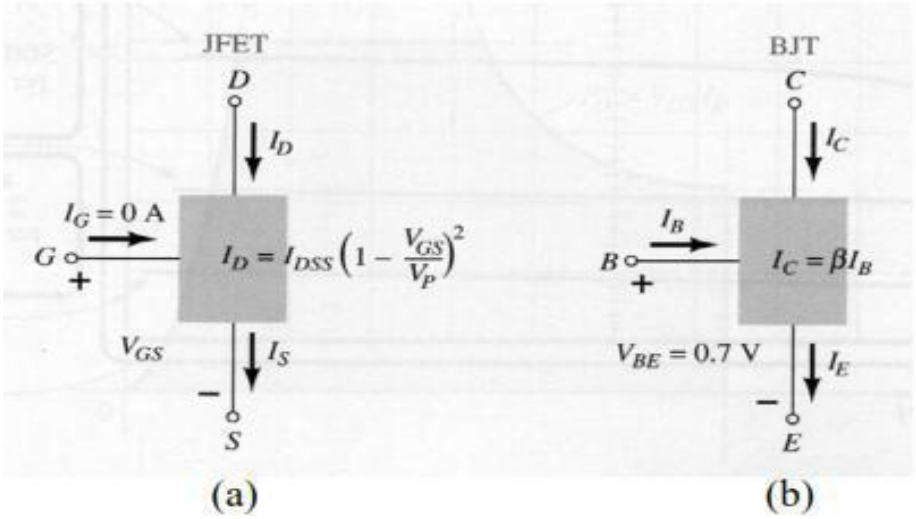


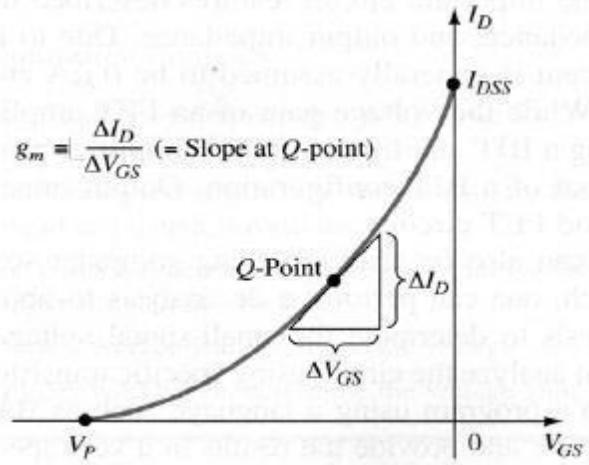
Fig.(1-10)

JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0A$	$\Leftrightarrow$	$V_{BE} \cong 0.7V$

Transconductance Factor:

The change in drain current that will result from a change in gate-to-source voltage can be determined using the transconductance factor gm in the following manner:

$$\Delta I_D = g_m \cdot \Delta V_{GS}$$



The transconductance factor, gm,)on specification sheets, gm is provided as yfs) is the slop of the characteristics at the point of operation, as shown in Fig. 1-11.

Fig.(1-11)

That is,

$$g_m = y_{fs} = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=const.}$$

An equation for gm can be derived as follows:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q-pt.} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2\right] = I_{DSS}\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$g_m = 2I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right) = 2I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]\left[0-\frac{1}{V_P}\right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1-\frac{V_{GS}}{V_P}\right] \qquad \textbf{[1.2]}$$

And

$$g_{m_o} = \frac{2I_{DSS}}{|V_P|} \qquad \textbf{[1.3]}$$

where g mo is the value of gm at VGS = 0 V. Equation [1.2] then becomes:

$$g_m = g_{m_o}\left[1-\frac{V_{GS}}{V_P}\right] \qquad \textbf{[1.4]}$$

JFET Output Impedance:

The output impedance (rd) is defined on the drain (output) characteristics of Fig. 1-12 as the slope of the horizontal characteristic curve at the point of operation. In equation form:

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=const.} \qquad \textbf{[1.5]}$$

where y_{os} is the output admittance, with the units of μS.

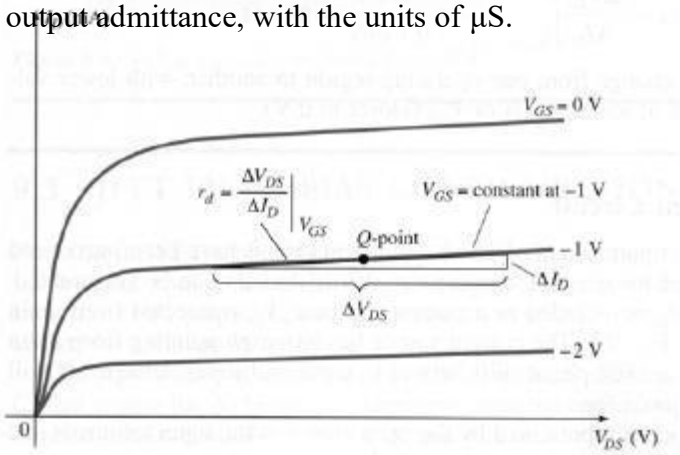


Fig.[1-12]

MOSFET

1. DEPLETION-TYPE MOSFET

There are two types of FETs: JFETs and MOSFETs. MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor. Since there are differences in the characteristics and operation of each type of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which happens to have characteristics similar to those of a JFET between cutoff and saturation at I_{DSS} but then has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. (1-1).

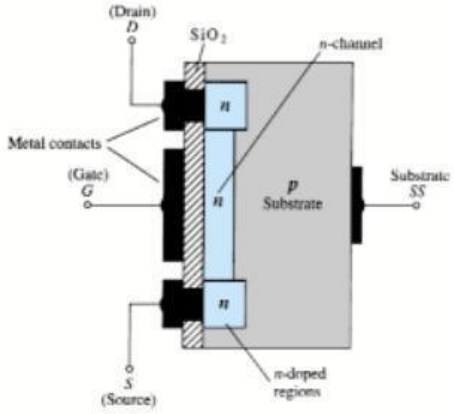


Fig. (1-1)

- There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

- It is the insulating layer of SiO in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics

In Fig. 1-2 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with V_{GS} =0 V continues to be labeled I_{DSS}, as shown in Fig. 1-3.

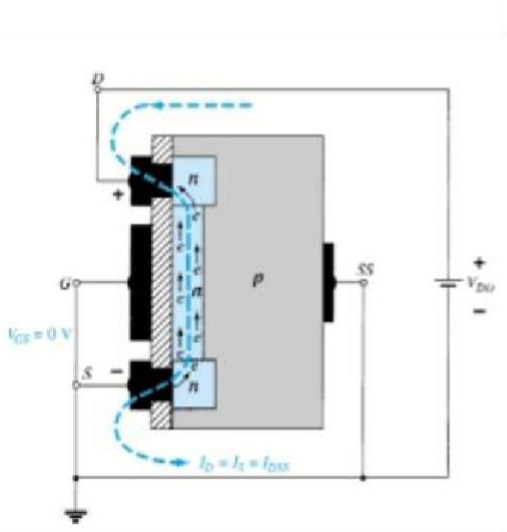


Fig. (1-2)

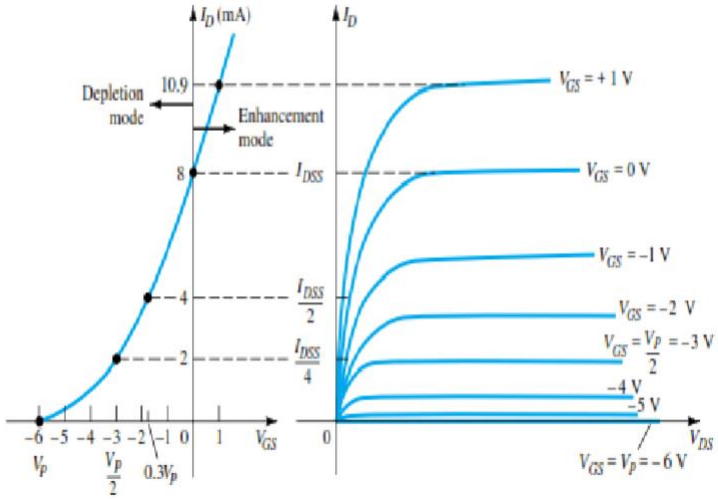


Fig.(1-3)

In Fig. 1-4, V_{GS} has been set at a negative voltage such as 1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 1-4. Depending on the magnitude of the negative bias established by V_{GS} , a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown in Fig. 1-3 for V_{GS}= 1 V, 2 V, and so on, to the pinch-off level of 6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.

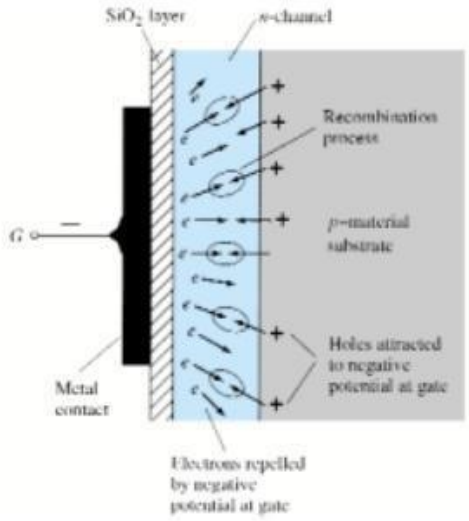


Fig.(1-4)

Example

Sketch the transfer characteristics for an n-channel depletion-type MOSFET with I_{DSS} =10 mA and VP =4V

Solution

At $V_{GS} = 0$ V, $I_D = I_{DSS} = 10$ mA

$V_{GS} = V_P = -4$ V, $I_D = 0$ mA

$$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2\text{ V}, \qquad I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5\text{ mA}$$

and at $I_D = \frac{I_{DSS}}{2}$, $V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$

all of which appear in Fig. 1-5.Before plotting the positive region of V_{GS}

, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values

to be substituted into Shockley's equation. In this case, we will try 1 V as follows:

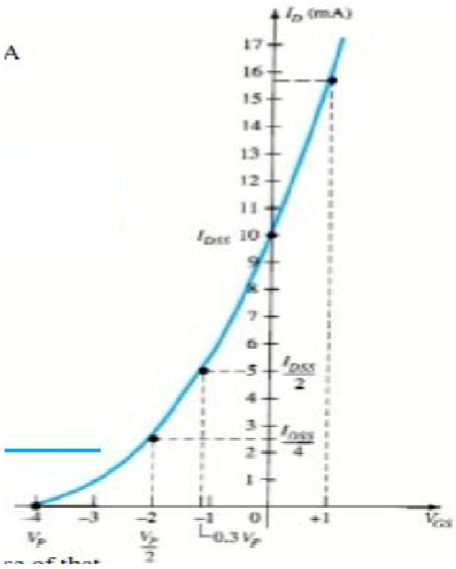
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = 10\text{ mA}$$

$$\cong 15.63\text{ mA}$$

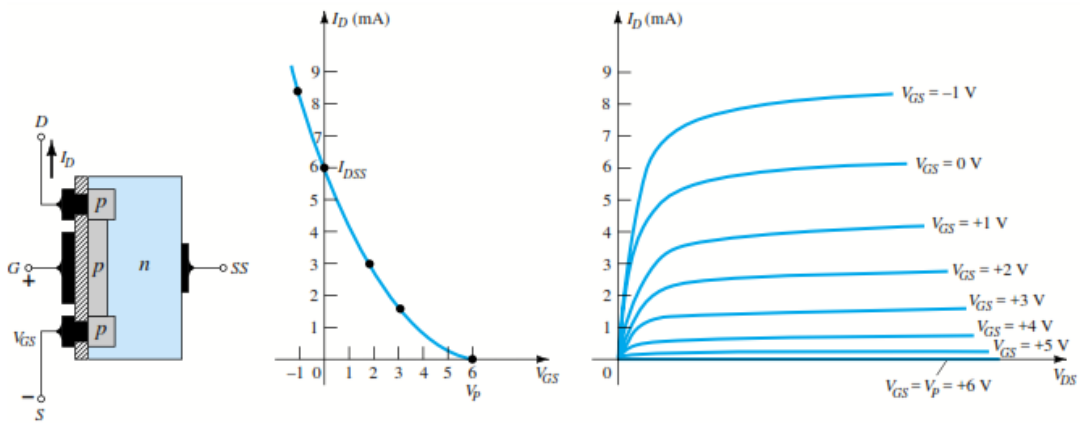
which is sufficiently high to finish the plot.

Fig.(1-5)



p-Channel Depletion-Type MOSFET

The construction of a p-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 1-1. That is, there is now an n-type substrate and a p-type channel, as shown in Fig. 1-6a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure.



(a) **(b)** **(c)**

Fig. (1-6)

Symbols of n-channel and p-channel MESFET are shown in Fig.(1-7).

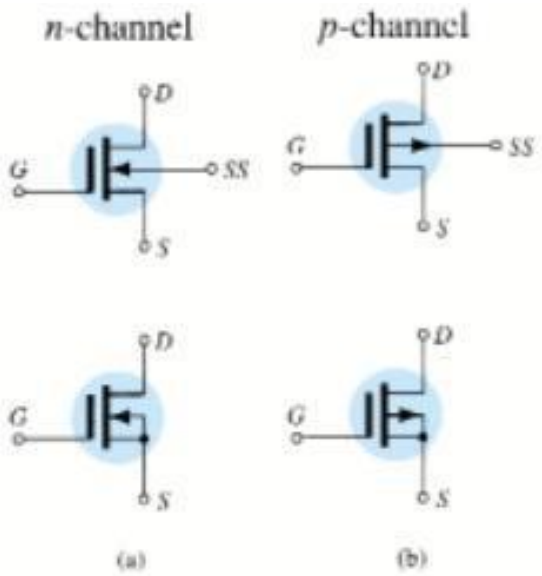


Fig. (1-7)

2. ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an n-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for n-channel JFETs and n-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig. 2-1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate.

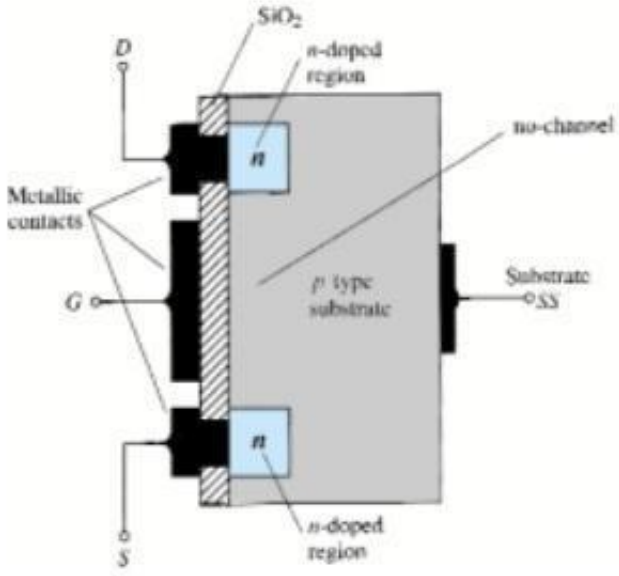


Fig. (2-1)

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 2-1, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes — quite different from the depletion-type MOSFET and JFET where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V at 0 V, and terminal directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

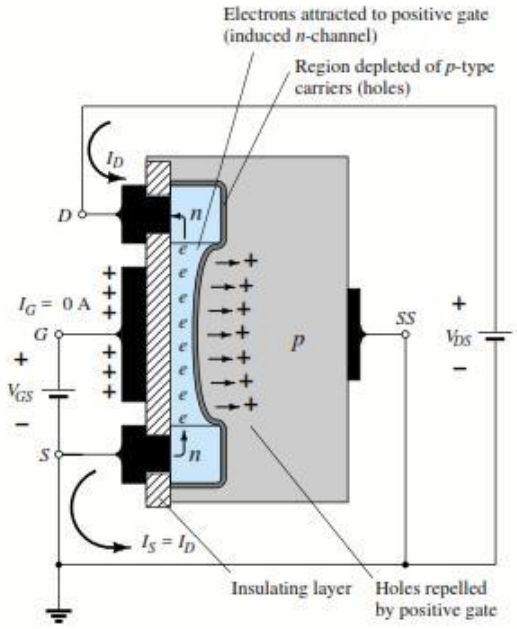


Fig. (2-2)

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS} , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_{DDS} is due

to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 2-3. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 2-3, we find that

VDG=VDS- VGS

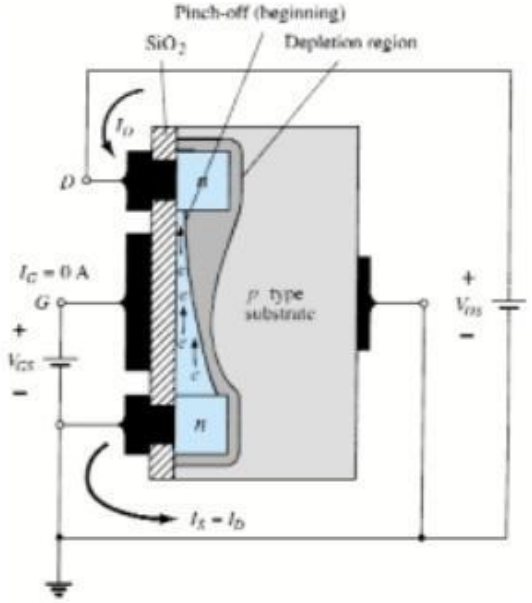


Fig. (2-3)

In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by:

$$V_{DS_{sat}} = V_{GS} - V_T$$

Obviously, therefore, for a fixed value of V_T , then the higher the level of V_{GS} , the more the saturation level for V_{DS}, as shown in Fig. 2-3 .

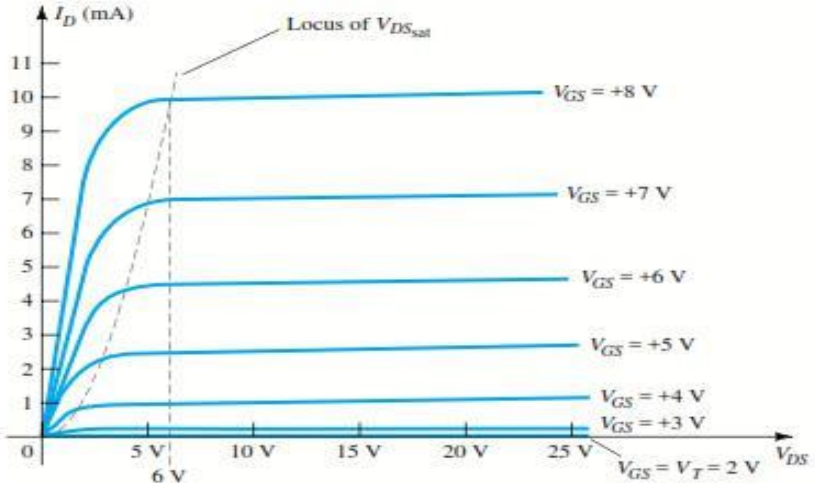


Fig.(2-4)

- **For values of VGS less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.**

Figure 2-4 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increased as the magnitude of V_{GS} increased, resulting in ever-increasing increments in drain current. For levels of $V_{GS}>V$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

Symbols of Enhancement MOSFET of P-channel and n-channel are shown in Fig. (2-5).

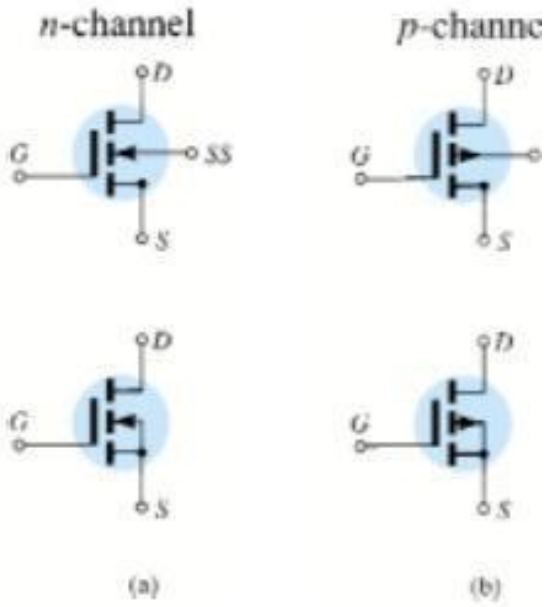


Fig.(2-5)

MOSFET Small Signal Analysis

1. DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in Fig. 1-1.The only difference offered by D-MOSFETs is that V_{GSQ} can be positive for n-channel devices and negative for p-channel units. The result is that g_m can be greater than g_{m0} as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

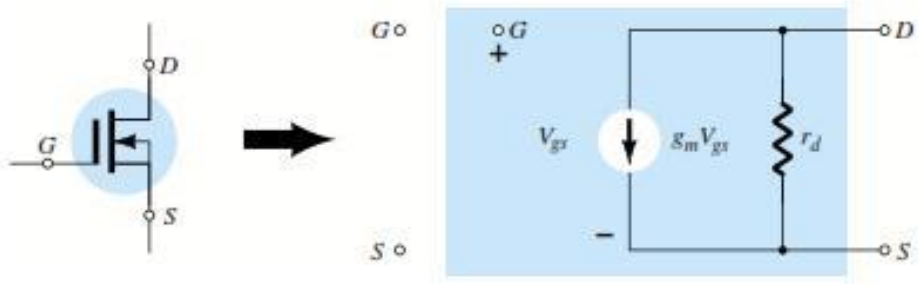


Fig.(1-1)

2. Enhancement-TYPE MOSFETs:

The enhancement-type MOSFET can be either an n-channel (nMOS) or p-channel (pMOS) device, as shown in Fig. 2-1. The ac small-signal equivalent circuit of either device is shown in Fig. 2-1,revealing an open-circuit between gate and drain source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source r_d, which is usually provided on specification sheets as an admittance y_{os}. The device transconductance, g_m, is provided on specification sheets as the forward transfer admittance, y_{fs}.

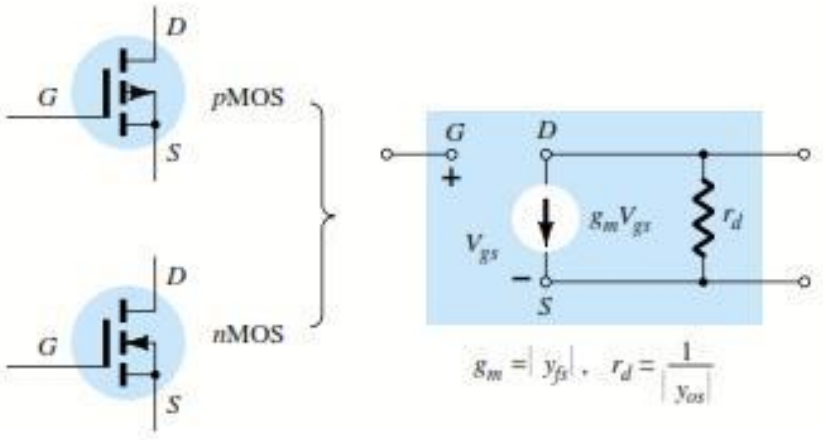


Fig.(2-1)

In our analysis of JFETs, an equation for g_m was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})}$$

ANALOG Vs DIGITAL:

To learn and understand about the digital logic design, the initial knowledge we require is to differentiate between analog and digital. The following are fews that differentiate between analog and digital.

- Analog information is made up of a continuum of values within a given range.

- At its most basic, digital information can assume only one of two possible values: one/zero, on/off, high/low, true/false, etc.
- Digital Information is less susceptible to noise than analog information
- Exact voltage values are not important, only their class (1 or 0)
- The complexity of operations is reduced, thus it is easier to implement them with high accuracy in digital form.

DIGITAL SYSTEMS

Digital means electronic technology that generates, stores, and processes data in terms of two states: positive and non-positive. Positive is expressed or represented by the number 1 and non-positive by the number 0.

A „**digital system**" is a data technology that uses discrete (discontinuous) values represented by high and low states known as bits. By contrast, non-digital (or analog) systems use a continuous range of values to represent information. Although digital representations are discrete, the information represented can be either discrete, such as numbers, letters or icons, or continuous, such as sounds, images, and other measurements of continuous systems.

BINARY

Binary describes a numbering scheme in which there are only two possible values for each digit: 0 and 1. The term also refers to any digital encoding/decoding system in which there are exactly two possible states. In digital data memory, storage, processing, and communications, the 0 and 1 values are sometimes called "low" and "high," respectively.

BINARY NUMBER/BINARY NUMBER SYSTEM

The binary number system is a numbering system that represents numeric values using two unique digits (0 and 1). Most of the computing devices use binary numbering to represent electronic circuit voltage state, (i.e., on/off switch), which considers 0 voltage input as off and 1 input as on.

This is also known as the base-2 number system (The base-2 system is a positional notation with a radix of 2), or the binary numbering system. Few examples of binary numbers are as follows:

- 10
- 111
- 10101
- 11110

COMPLIMENTS

Compliments are used in digital computers to simplify the subtraction operation and for logical manipulation. Simplifying operations leads to simpler, less expensive circuits to implement the operations.

There are 2 types of complements for each base r system.

(1) The radix complement
(2) Diminished radix compliment

Radix compliment: Also referred to as the r‟s compliment.

Diminished radix compliment: Also referred to as (r-1)‟s compliment.

OCTAL NUMBERS

The **Octal Number System** is another type of computer and digital base number system. The **Octal Numbering System** is very similar in principle to the previous hexadecimal numbering system except that in Octal, a binary number is divided up into groups of only 3 bits, with each group or set of bits having a distinct value of between 000 (0) and 111 (7). Octal numbers therefore have a range of just “8” digits, (0, 1, 2, 3, 4, 5, 6, 7) making them a Base-8 numbering system and therefore, q is equal to “8”.

HEXADECIMAL NUMBERING SYSTEM: The one main disadvantage of binary numbers is that the binary string equivalent of a large decimal base-10 number can be quite long. When working with large digital systems, such as computers, it is common to find binary numbers consisting of 8, 16 and even 32 digits which makes it difficult to both read and write without producing errors especially when working with lots of 16 or 32-bit binary numbers. One common way of overcoming this problem is to arrange the binary numbers into groups or sets of four bits (4-bits). These groups of 4-bits uses another type of numbering system also commonly used in computer and digital systems called **Hexadecimal Numbers**

The “Hexadecimal” or simply “Hex” numbering system uses the **Base of 16** system and are a popular choice for representing long binary values because their format is quite compact and much easier to understand compared to the long binary strings of 1‟s and 0‟s.

Being a Base-16 system, the hexadecimal numbering system therefore uses 16 (sixteen) different digits with a combination of numbers from 0 through to 15. In other words, there are 16 possible digit symbols.

Decimal	Binary	Octal	Hexadecimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

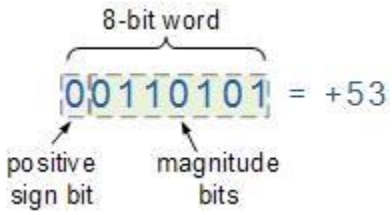
SIGNED BINARY NUMBERS

In mathematics, positive numbers (including zero) are represented as unsigned numbers. That is we do not put the +ve sign in front of them to show that they are positive numbers. However, when dealing with negative numbers we do use a -ve sign in front of the number to show that the number is negative in value and different from a positive unsigned value and the

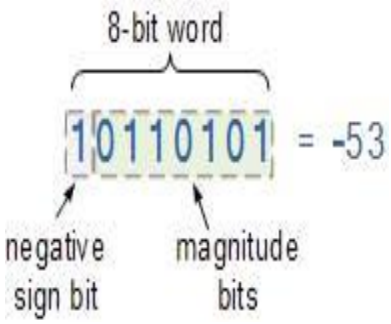
same is true with **signed binary numbers**. However, in digital circuits there is no provision made to put a plus or even a minus sign to a number, since digital systems operate with binary numbers that are represented in terms of "0"s" and "1"s".

So to represent a positive (N) and a negative (-N) binary number we can use the binary numbers with sign. For signed binary numbers the most significant bit (MSB) is used as the sign. If the sign bit is "0", this means the number is positive. If the sign bit is "1", then the number is negative. The remaining bits are used to represent the magnitude of the binary number in the usual unsigned binary number format.

Positive Signed Binary Numbers.



Negative Signed Binary Numbers



DeMorgan's Theory :

As we have seen previously, Boolean Algebra uses a set of laws and rules to define the operation of a digital logic circuit with "0's" and "1's" being used to represent a digital input or output condition. Boolean Algebra uses these zeros and ones to create truth tables and mathematical expressions to define the digital operation of a logic AND, OR and NOT (or inversion) operations as well as ways of expressing other logical operations such as the XOR (Exclusive-OR) function.

While George Boole's set of laws and rules allows us to analyise and simplify a digital circuit, there are two laws within his set that are attributed to **Augustus DeMorgan** (a nineteenth century English mathematician) which views the logical NAND and NOR operations as separate NOT AND and NOT OR functions respectively.

But before we look at **DeMorgan's Theory** in more detail, let's remind ourselves of the basic logical operations where A and B are logic (or Boolean) input binary variables, and whose values can only be either "0" or "1" producing four possible input combinations, 00, 01, 10, and 11.

Truth Table for Each Logical Operation

Input Variable		Output Conditions				
A	B	AND	NAND	OR	NOR	EXOR
0	0	0	1	0	1	0
0	1	0	1	1	0	1
1	0	0	1	1	0	1

1	1	1	0	1	0	0

The following table gives a list of the common logic functions and their equivalent Boolean notation where a "." (a dot) means an AND (product) operation, a "+" (plus sign) means an OR (sum) operation, and the complement or inverse of a variable is indicated by a bar over the variable.

Logic Function	Boolean Notation
AND	A.B
OR	A+B
NOT	A
NAND	A .B
NOR	A+B
EXOR	A ⊕ B (or) AB' + A'B

DeMorgan's laws:

DeMorgan's Theorems are basically two sets of rules or laws developed from the Boolean expressions for AND, OR and NOT using two input variables, A and B. These two rules or

theorems allow the input variables to be negated and converted from one form of a Boolean function into an opposite form.

DeMorgan's first theorem states that two (or more) variables NOR´ed together is the same as the two variables inverted (Complement) and AND´ed, while the second theorem states that two (or more) variables NAND´ed together is the same as the two terms inverted (Complement) and OR´ed. That is replace all the OR operators with AND operators, or all the AND operators with an OR operators.

DeMorgan's First Theorem

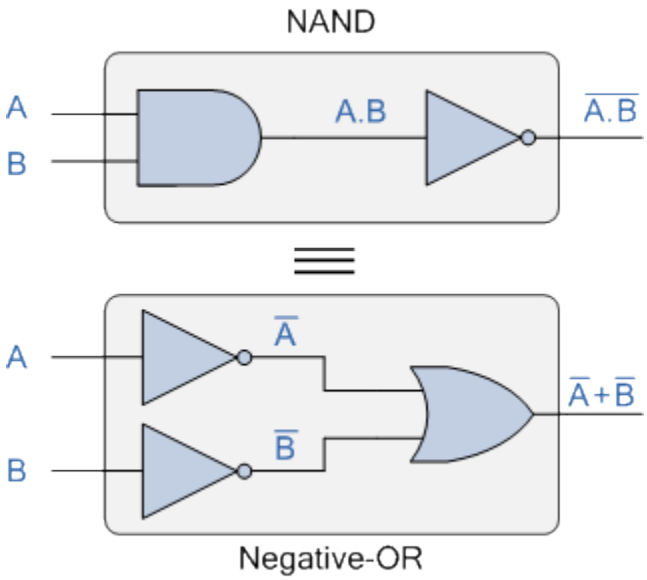
DeMorgan's First theorem proves that when two (or more) input variables are AND'ed and negated, they are equivalent to the OR of the complements of the individual variables. Thus the equivalent of the NAND function and is a negative-OR function proving that A.B = A+B and we can show this using the following table.

Verifying DeMorgan's First Theorem using Truth Table

Inputs		Truth Table Outputs For Each Term				
B	A	A.B	A.B	A	B	A + B
0	0	0	**1**	1	1	**1**
0	1	0	**1**	0	1	**1**
1	0	0	**1**	1	0	**1**
1	1	1	**0**	0	0	**0**

We can also show that A.B = A+B using logic gates as shown.

DeMorgan's First Law Implementation using Logic Gates



The top logic gate arrangement of: A.B can be implemented using a NAND gate with inputs A and B. The lower logic gate arrangement first inverts the two inputs producing A and B which become the inputs to the OR gate. Therefore the output from the OR gate becomes: A+B

Thus an OR gate with inverters (NOT gates) on each of its inputs is equivalent to a NAND gate function, and an individual NAND gate can be represented in this way as the equivalency of a NAND gate is a negative-OR.

DeMorgan's Second Theorem

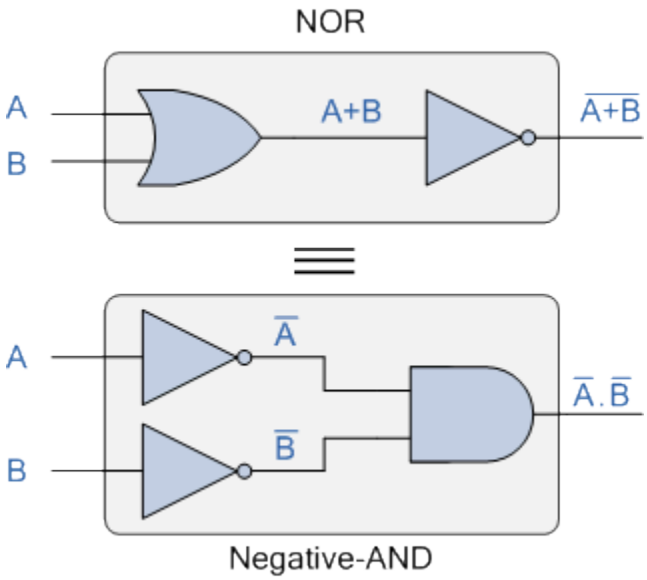
DeMorgan's Second theorem proves that when two (or more) input variables are OR'ed and negated, they are equivalent to the AND of the complements of the individual variables. Thus the equivalent of the NOR function and is a negative-AND function proving that A+B = A.B and again we can show this using the following truth table.

Verifying DeMorgan's Second Theorem using Truth Table

Inputs		Truth Table Outputs For Each Term				
B	A	A+B	A+B	A	B	A . B
0	0	0	**1**	1	1	**1**
0	1	1	**0**	0	1	**0**
1	0	1	**0**	1	0	**0**
1	1	1	**0**	0	0	**0**

We can also show that A+B = A.B using logic gates as shown.

DeMorgan's Second Law Implementation using Logic Gates



The top logic gate arrangement of: A+B can be implemented using a NOR gate with inputs A and B. The lower logic gate arrangement first inverts the two inputs producing A and B which become the inputs to the AND gate. Therefore the output from the AND gate becomes: A.B

Thus an AND gate with inverters (NOT gates) on each of its inputs is equivalent to a NOR gate function, and an individual NOR gate can be represented in this way as the equivalency of a NOR gate is a negative-AND.

Although we have used DeMorgan's theorems with only two input variables A and B, they are equally valid for use with three, four or more input variable expressions, for example:

For a 3-variable input

A.B.C = A+B+C

and also

A+B+C = A.B.C

For a 4-variable input

A.B.C.D = A+B+C+D

and also

A+B+C+D = A.B.C.D

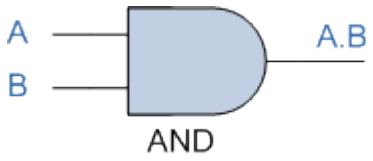
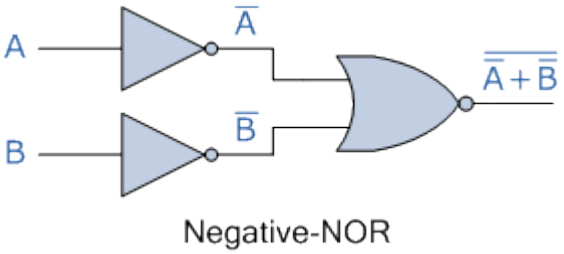
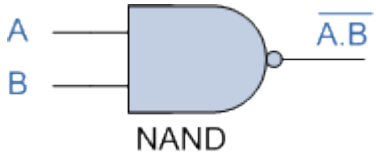
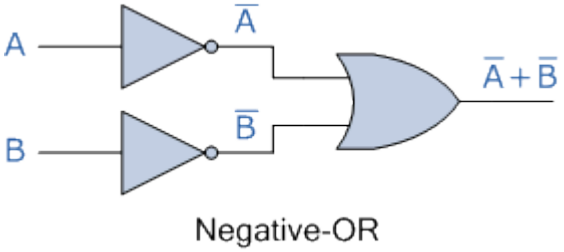
and so on.

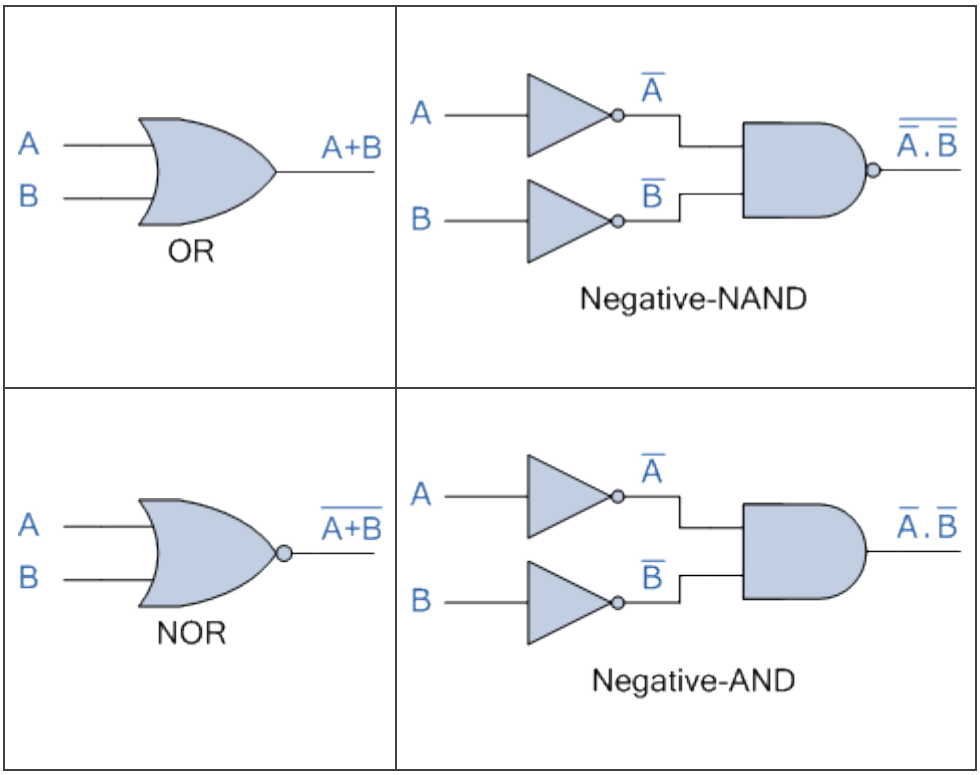
DeMorgan's Equivalent Gates

We have seen here that DeMorgan's Theorems replace all of the AND (.) operators with OR (+) and vice versa and then complements each of the terms or variables in the expression by inverting it, that is 0's to 1's and 1's to 0's before inverting the entire function.

Thus to obtain the DeMorgan equivalent for an AND, NAND, OR or NOR gate, we simply add inverters (NOT-gates) to all inputs and outputs and change an AND symbol to an OR symbol or change an OR symbol to an AND symbol as shown in the following table.

DeMorgan's Equivalent Gates

Standard Logic Gate	DeMorgan's Equivalent Gate
	
	

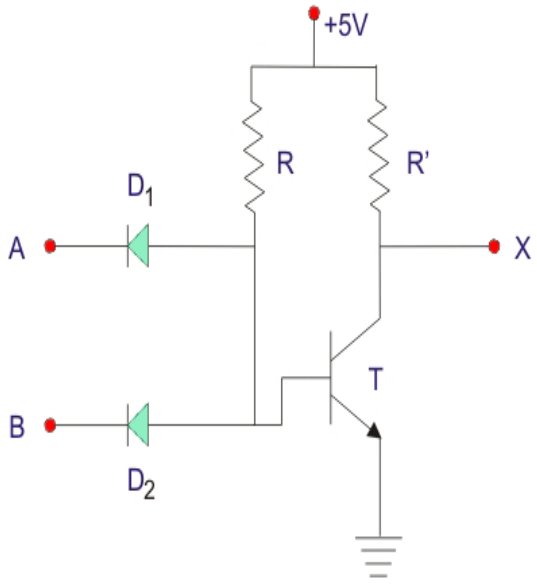


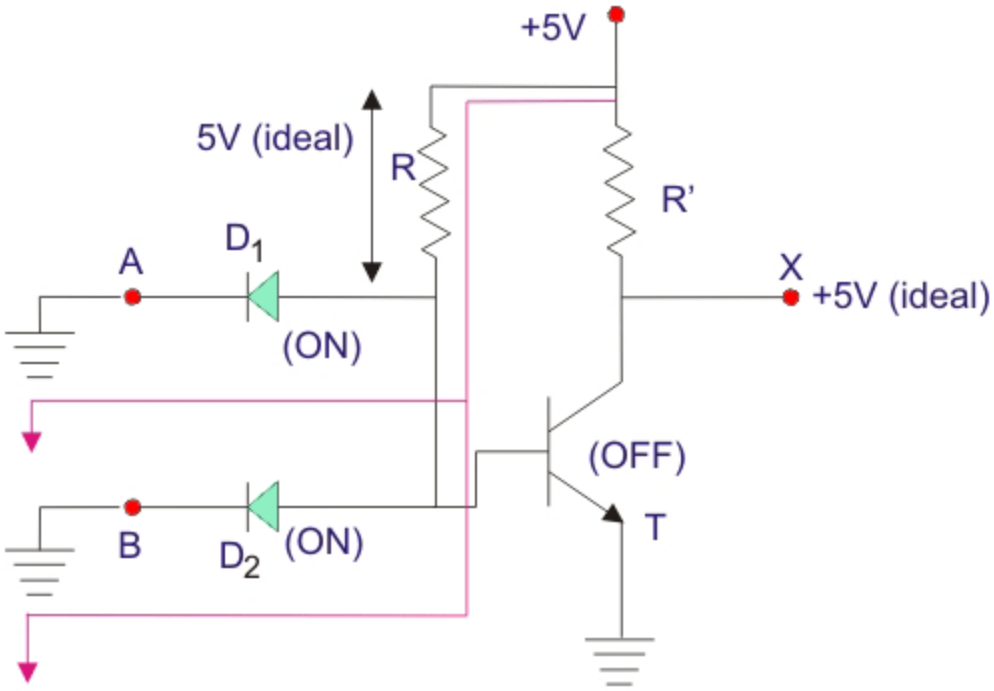
Then we have seen that the complement of two (or more) AND'ed input variables is equivalent to the OR of the complements of these variables, and that the complement of two(or more) OR'ed variables is equivalent to the AND of the complements of the variables as defined by *DeMorgan*.

Realizing NAND Gate using Diode and Transistor

For simplicity we will show here only two inputs NAND gate circuit by using diodes and transistors. This NAND gate is called **DTL NAND gate** or **Diode Transistor Logical NAND Gate**.

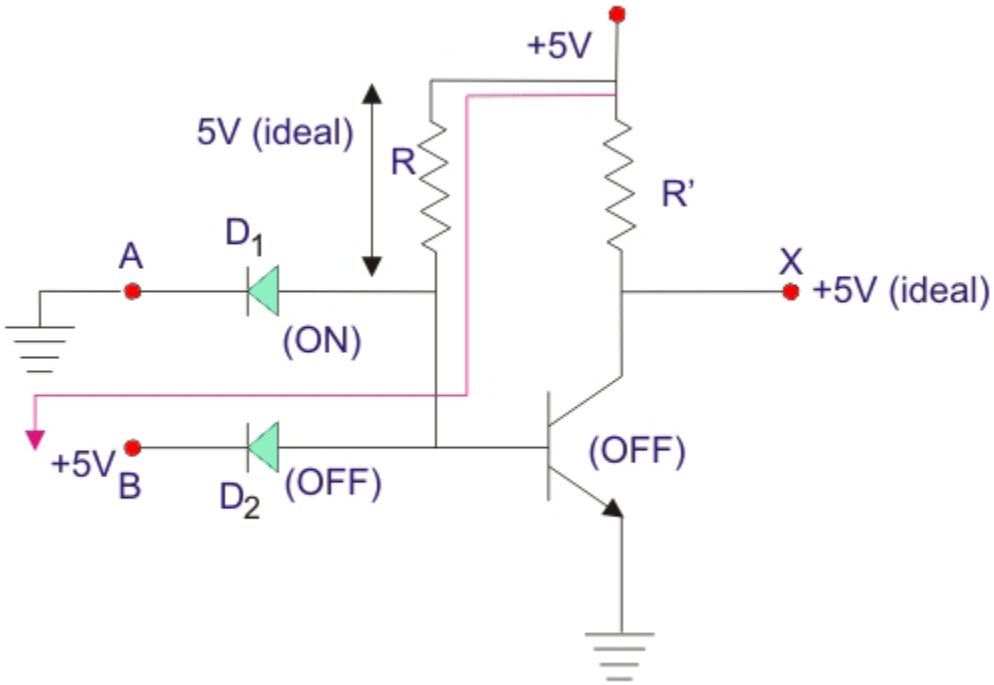
When both input A and B are given with 0 V, both of the diodes are in forward biased condition that is in ON condition. Supply voltage will get path to the ground through diode D_1 and D_2. Entire supply voltage +5 V will ideally drop across resistor R and hence base terminal of transistor T will not get enough potential to turn ON the transistor and hence the transistor will be in OFF condition. As a result supply voltage +5 V will appear at output terminal X and hence output X will become high or logical 1.

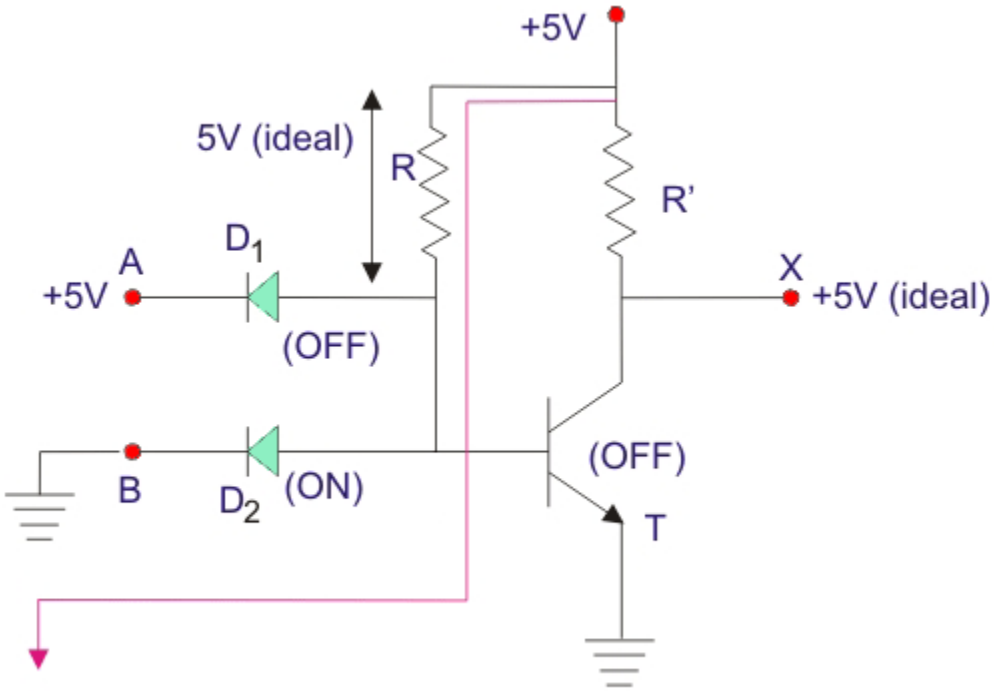




Now if either of diode D_1 and D_2, is applied with 0 V, the same thing happens as in these cases also the supply voltage gets a path to the ground either of the forward biased diode. In that cases

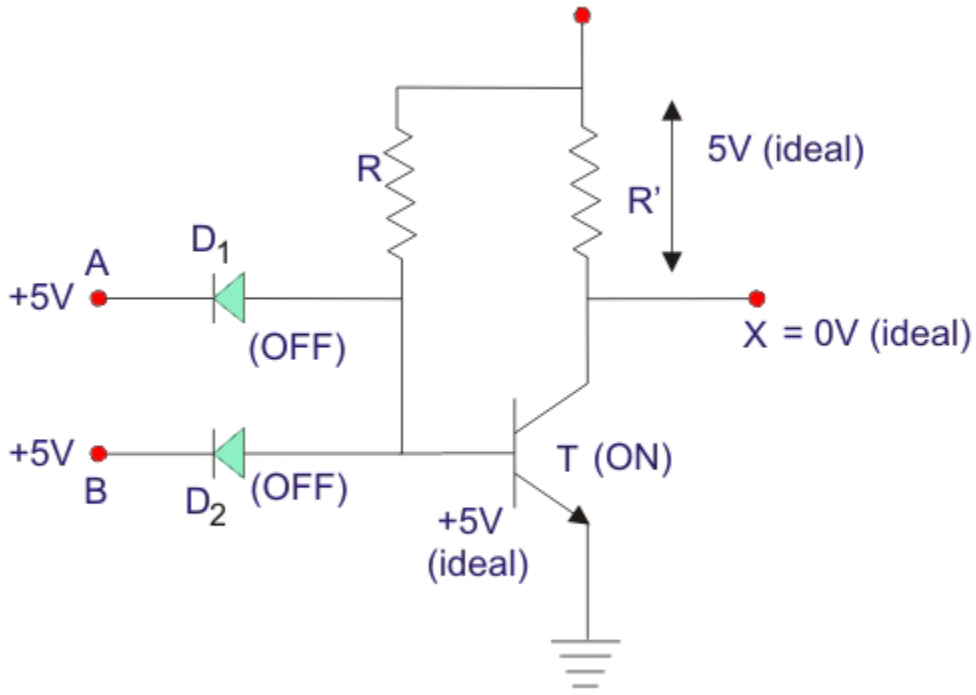
also the output will be logical high or 1.





When both of the inputs are given with +5 V that is logical 1, both of the diodes are in OFF condition and hence supply voltage will appear at the base terminal of the transistor T which makes it switched ON and supply voltage gets a path to the ground through this transistors. Ideally entire supply voltage +5 V will drop across resistor R' and output terminal X will get ideally zero volts

and hence the output is considered as logical 0. Hence, the output is only 0 when and only when both inputs are +5 V or logical 1.



SAMPLING GATES AND LOGIC GATES

IC families:

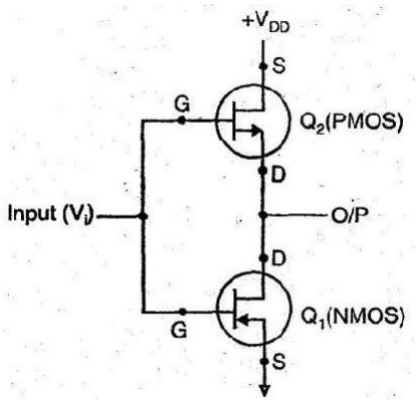
comparison of the important characteristics of various IC logic families.

	Parameter	RTL	I^2L	DTL	HTL	TTL	ECL	MOS	CMOS
1.	Basic Gate	NOR	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR or NAND
2.	Fan-out	5	Depends on injector current	8	10	10 to 20	25	20	20 to 50
3.	Power dissip-ation in mW	12	6mm to 70 µM	8-12	55	10	40-55	0.2-10	0.0025
4.	Noise immunity	Nominal	Poor	Good	Excellent	Very Good	Poor	Good	Very Good
5.	Propagation delay (in sec.)	12	25-250	30	90	10	0.75	300	70.0
6.	Clock rate (MHZ)	8	–	72	4	35	>60	2	10
7.	Available functions	High	LSI only	Fairly high	Nominal	Very high	High	low	High

(i) CMOS inverter

(ii) Tristate logic

(i) CMOS Inverter: It is complementary MOSFET obtained by using P-channel MOSPET and n-channel MOSFET simultaneously. The P and N channel are connected in series, their drains are connected together, output is taken from common drain point. Input is applied at common gate terminal. CMOS is very fast and consumes less power.



Case 1. When input Vi = 0. The V_{GS} (Gate source) voltage of Q1 will be 0 volt, it will be off. But Q2 will be ON; Hence output will be equal to +VDD or logic 1.

Case 2. When input Vi = 1, The V_{GS} (Gate source) voltage of Q2 will be 0 volt, it will be OFF, But Q1 will be ON. Hence output will be connected to•
ground or logic 0.

In this way, CMOS function as an inverter.

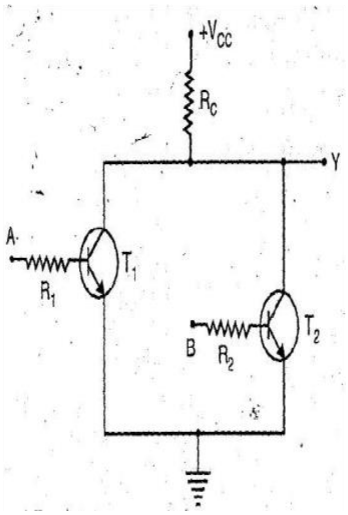
(ii) Tri-state logic: When there are three states i.e. state 0, state 1 and high impendence i.e. called Tri-state logic. High impedance is considered as state when no current pass through circuit. Although in state 0 and state 1 circuit functions and current flows through it.

- Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit.
- Fan-in is the number of inputs to the gate which it can handle.
- Fan-out is the number of loads the output of a gate can drive without effecting its operation.
- Power dissipation is the supply voltage required by the gate to operate with 50% duty cycle at a given frequency
- RTL, DTL, DTL are the logic families which are now obsolete.
- TTL is the most widely used logic family.

- TTL gates may be:
  (a) Totem pole
  (b) Open collector
  (c) Tri-state .
- TTL is used in SSI and MSI Integrated circuits and is the fastest of all standard logic families.
- Totem pole TTL has the advantage of high speed and low power dissipation but its disadvantage is that it cannot be wired ANDed because of current spikes generation.
- Tri-state has three states : .
  (a) High
  (b) Low
  (c) High Impedance
- ECL is the fastest of all logic families because its propagation delay is very small i.e. of about 2 nsec.
- ECL can be wired ORed.
- MOS logic is the simplest to fabricate.
- MOS transistor can be connected as a resistor.
- MOSFET circuitry are normally constructed from NMOS devices because they are 3 times faster than PMOS devices.
- CMOS uses both P-MOS and N-MOS.
- CMOS needs less power as compared to ECL as they need maximum power.
- Both NMOS and PMOS are more economical than CMOS because of their greater packing densities.
- Speed of CMOS gates increases with increase in VDD.
- CMOS has large fan-out because of its low output resistance.

Schematic of RTL NOR gate and explain its operation.

RTL was the first to introduced. RTL NOR gate is as shown in fig.



Working:

Case I: When A = B = 0.

Both T1 and T2 transistors are in cut off state because the voltage is insufficient to drive the transistors i.e. VBE < 0.6 V: Thus, output Y will be high, approximately equal to supply voltage Vcc. As no current flows through Rc and drop across Rc is also zero.

Thus, Y = 1, when A = B = 0.

Case II : When A = 0 and B = 1 or A = 1 and B = 0.

The transistor whose input is high goes into saturation where as other will goes to off cut state. This positive input to transistor increases the voltage drop across the collector resistor and decreasing the positive output voltage.

Thus, Y = 0,when A= 0 and B = 1 or A = 1 and B = 0.

Case III : When A = B = 1**.** Both the transistors T1 and T2 goes into saturation and output voltage is equal to saturation voltage.

Thus, Y = 0,when A = B = 1

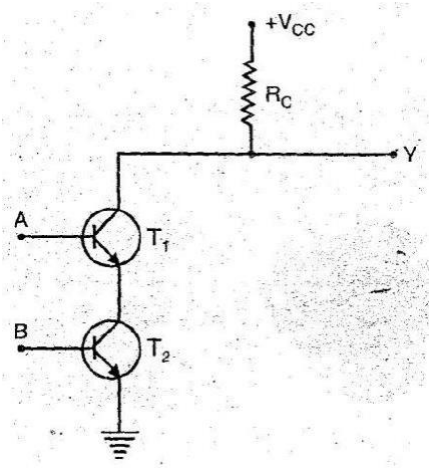
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Which is the output of NOR gate.

DCTL NAND gate with the help of suitable circuit diagram.

DCTL NAND gate circuit diagram is as shown:



Working

Case I: When A = B = 0. Both transistors T1 and T2 goes to cut off state. As the voltage is not sufficient to drive the transistor into saturation. Thus, the output voltage equal to Vcc. When A = B = 0, output Y = 1

Case II: When A = 0 and B = 1 or A = 1 and, B = 0. The corresponding transistor goes to cut off state and the output voltage equals to Vcc.

Thus, When A = 0 and B = 1 or A = 1 and B = 0, Output Y = 1.

Case III: When A = B = 1. Both transistors T1 and T2 goes into saturation state and output voltage is insufficient to consider as '1'

Thus when A B = 1, output Y = 0.

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Which is the output of NAND gate.

Compare standard TTL, Low power TTL and high speed TTL logic families.

Name of the Logic Family	Propagation Delay (ns)	Power Dissipation (mW)	Fan out	Max. Clock Rate (MHz)
1. Standard TTL	9	10	10	35
2. Low power TTL	33	1	20	3
3. High sped TTL	6	23	10	50

characteristics and specification of CMOS.

1 Power supply (VDD) = 3 — 15 Volts

2. Power dissipation (Pd) = 10 nW

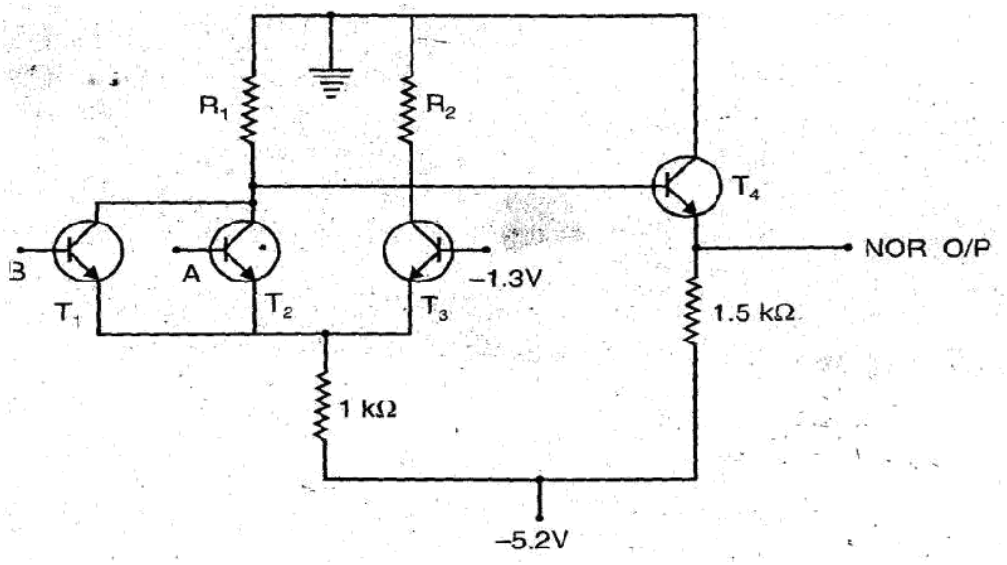
3. Propagation delay (td) = 25 ns

4. Noise margine (NM) = 45% of

VDD 5, Fan out (FO) = >50

Two input ECL NOR gate

The circuit diagram of two input ECL NOR gate is as shown

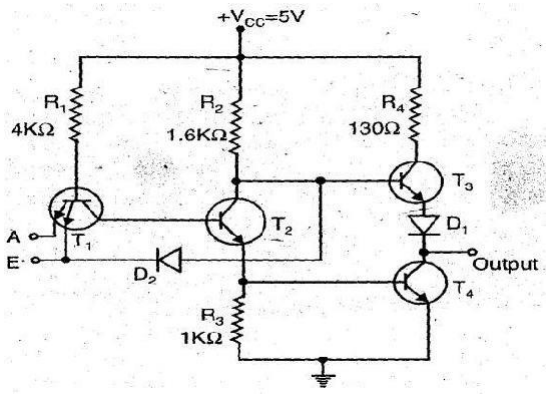


Working

Case I : When A = B = 0, the reference voltage of T3 is more forward biased then T1 and T2. Thus, T3 is ON and T1, T2 remains OFF. The value of R1 is such-that the output of NOR gate is high .i.e. '1'.

Case II: When A = 1 or B = 1 or A = B = 1, the corresponding transistors are ON, as they are more forward biased that T3 and thus T3 is OFF. Which makes the NOR output to be low i.e. '0'. This shows that the circuit works as a NOR gate.

TTL inverter.



Tristate TTL inverter utilizer the high-speed operation of totem-pole arrangement while permitting outputs to be wired ANDed (connected together). It is called tristate TTL because it allows three possible output stages. HIGH, LOW and High-Impedance. We know that transistor T3 is ON when output is HIGH and T4 is ON when output is LOW. In the high impedance state both transistors, transistor T3 and T4 in the totem pole arrangement are med OFF. As a result the output is open or floating, it is neither LOW nor HIGH.

The above fig. shows the simplified tristate inverter. It has two inputs A and E. A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state-of the transistor T1 (either ON or OFF) depends on the logic input A and the additional component diode is open circuited as cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input the base-emitter junction of T is forward biased and as a result it turns ON. This shunts the current through R1 away from T2 making it OFF. As T2 is OFF, there is no sufficient drive for T4 conduct and hence T4 turns OFF. The LOW at ENABLE input also forward biases diode D2, which shunt the current away from the base of T3, making it OFF. In this way, when ENABLE output is LOW, both transistors are OFF and output is at high impedance state.

ECL OR gate

ECL or gate : Emitter-coupled logic (ECL) is the fastest of all logic families and thus it is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. (A) which has three parts. The middle part is the difference amplifier which performs the logic operation.

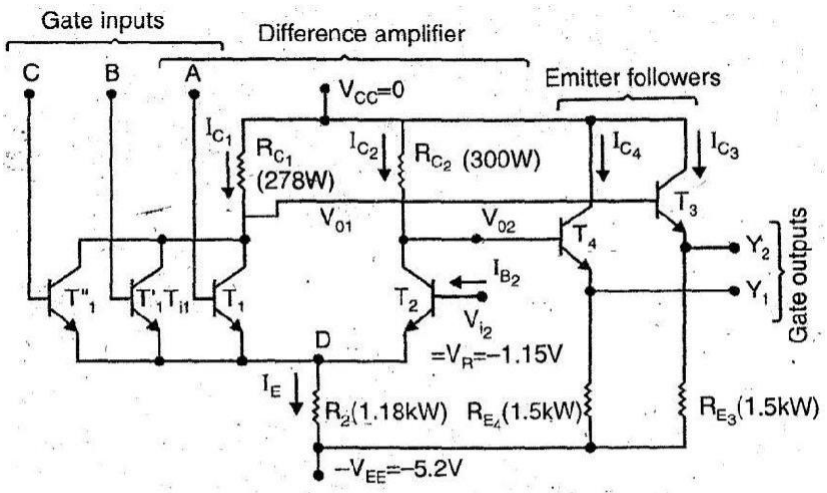


Fig. (A) A 3-input ECL OR/NOR Gate

Emitter followers are used for d.c. level shifting of the outputs, so that V (0) and V (1) are same for the inputs and the outputs. Note that two output Y1 and Y2 are available in this circuit which are complementary. Y1. corresponds to OR logic and Y2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply and protection of the gate from an accidental short circuit developing between the output of a gate and ground. The voltage corresponding to V (0) and V (1) are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. (B)

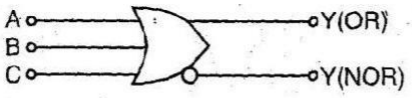
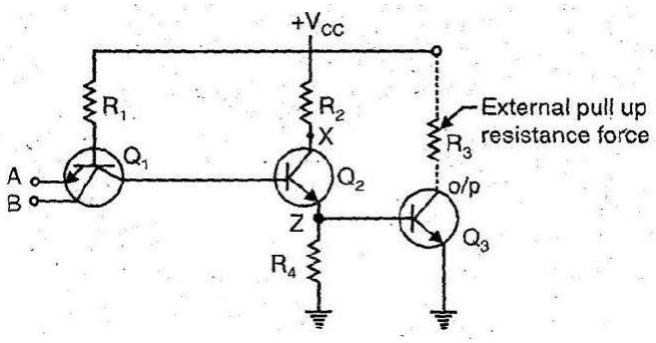


Fig. (B) The Symbol for a 3-input OR/NOR Gate

Open collector TTL NAND gate and explain its operation

The circuit diagram of 2-input NAND gate open-collector TTL gate is as shown:



Working:

Case.1 : When A = 0,B = 0

When both inputs A and B are low, both functions of Q1 are forward biased and Q2 remains off. So no current flows through R4 and Q3 is also off and its collector voltage is equal to Vcc i.e. Y = 1

Case2 : When A = 0, B = 1 and

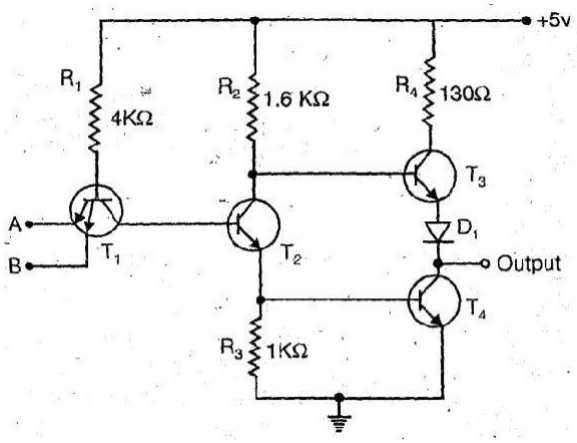
Case 3: When A = 1, B = 0

When one input is high and. other is low, then one junction is forward biased so Q2 is off and Q3 is also off. So collector voltage is equal to Vcc i.e. Y = 1 **Case 4**: When A = 1, B = 1

When both inputs are high, Q1 is turned off and Q2 turned 'ON' Q3 goes into saturation and hence Y = 0. The open-collector output has main advantage that wired ANDing is possible in it.

TTL NAND gate

Two input TTL NAND gate-is given in fig. (1). In this transistor T3 and T4 form a totem pole. Such type of configuration is called-as totem-pole output or active pull up output.



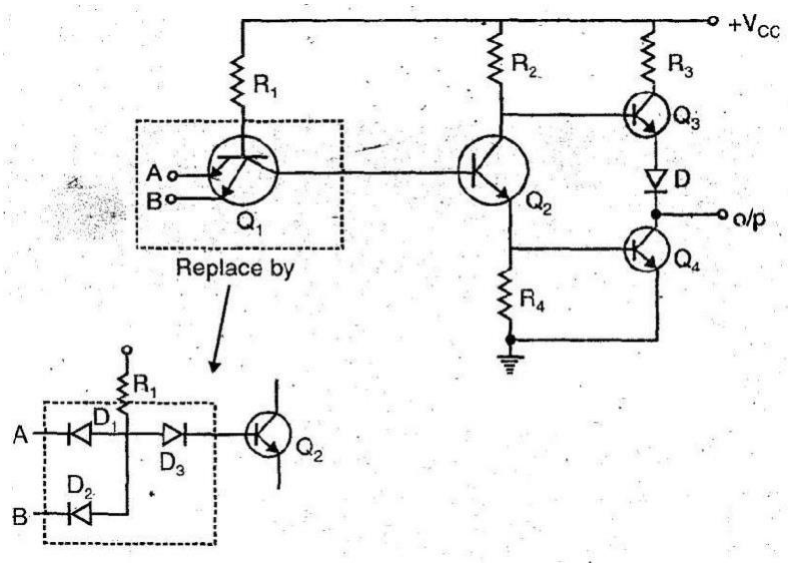
So, when A = 0 and B = 1 or (+5V). T1 conducts and T2 switch off. Since T2 is like an open switch, no current flows through it. But the current flows through the resistor R2 and into the base of transistor T3 to turn it ON. T4 remains OFF because there is no path through which it can receive base current. The output current flows through resistor R4 and diode D1. Thus, we get high' output.

When both inputs are high i.e. A = B = 1 or (+ 5V), T2 is ON and it drives T4 turning it ON. It is noted that the voltage at the base of T3 equals the sum of the base to emitter drop of T4 and $V_{CE\ (Sat)}$ of T2.

The diode D1 does not allow base-emitter junction of T3 to be forward-biased and hence, T3 remains OFF when T4 is ON. Thus, we get low output. It works as TTL NAND gate.

Totem pole NAND gate

In TTL Totem pole NAND gate, multiple emitter transistor as input is used. The no. of inputs may be from 2 to 8 emitters. The circuit diagram is as shown



Case 1:

When A = 0, B = 0

Now D1 and D2 both conduct, hence D3 will be off and make Q2 off. So its collector voltage rises and make Q3 ‘ON’ and Q4 off; Hence output at Y = 1 (High)

Case 2 and Case 3:

If A = 0, B = 1 and A = 1, B=0

In both cases, the diode corresponding to low input will conduct and hence diode P3 will be OFF making Q2 OFF. In a similar way its collector voltage rises Q3 ‘ON’ and Q4 ‘OFF’. Hence output voltage Y = 1 (High).

Case 4: A = 1, B = 1

Both diodes D1 and D2 will be off. D3 will be ‘ON’ and Q2 will ‘ON’ making Q4 also ‘ON’. But Q3 will be ‘OFF’. So output voltage Y = 0.

All the four cases shows that circuit operates as a NAND gate.

Totem pole can’t be Wired ANDed due to current spike problem. The transistors used in circuits may get damaged over a period of time though not immediately. Sometimes voltage level rises high than the allowable.